A Fast-Settling, High Dynamic Range
Fully Differential Operational Transconductance Amplifier

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Abstract

In this project, we have designed a fully-differential operational transconductance amplifier with capacitive feedback network producing a close-loop gain of 0.2. The OTA was designed in the single-stage telescopic topology and simulation with HSPICE and achieved a very fast settling time of less than 5ns and a settling accuracy of at least 0.2%. The OTA has the differential output swing of ±1.8V and a dynamic range greater than 85dB while consuming 7.2mW from a 3V supply for the main amplifier and 1.9mW for the bias network.

I. Design Approach and Decisions

Choosing the right overall circuit topology for a given set of specifications so as to avoid over-designing the circuit is one of the most critical design decisions to start out with. We begin investigating the specifications of the project very closely, and look at the pool of candidates for the best circuit topology. For the single-stage design, we consider telescopic, folded-cascode and gain-boosting amplifiers. Two-stage design consists of using a full 2-stage or a preamp followed by a full-stage amplifier. However, the fact that we only need 0.2% settling accuracy tells us that the open-loop gain for the OTA need not be extremely high (as shown later in Section III). In fact, an open-loop gain of more or less 1000 at around the maximum differential swing should suffice. Hence, to employ the design in a two-stage or gain-boosting topology may give excessive dc gain while dissipate much more power.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>Supply V(_{DD})</td>
<td>3V</td>
</tr>
<tr>
<td>Closed-loop gain, c</td>
<td>0.2</td>
</tr>
<tr>
<td>DR at output</td>
<td>≥ 85 dB</td>
</tr>
<tr>
<td>Settling accuracy</td>
<td>≤ 0.2%</td>
</tr>
<tr>
<td>Settling time, t(_s)</td>
<td>≤ 5 ns</td>
</tr>
<tr>
<td>Process</td>
<td>EE240 0.35um</td>
</tr>
<tr>
<td>Process corners</td>
<td>slow/nominal/fast</td>
</tr>
</tbody>
</table>

Table 1: Project specifications

![Conceptual diagram of amplifier configured as gain stage.](image)
Dynamic range of 85dB indicates that the OTA should be designed with large output swing range and that the integrator will need a large load capacitor at the output. A full two-stage design is the best candidate in terms of the output differential range, but the major drawback is the need for a minimum of four current legs (all drawing comparable currents) and thus may have big impact on the power consumption. At this point we decided to forego the 2-stage design.

In addition, a 5ns settling time is quite a stringent requirement and this makes the fast and simple single-stage telescopic or folded-cascode very attractive. The folded-cascode design suffers from the extra current leg introduced by the folded structure while only providing one extra $V_{ds\text{sat}}$ headroom advantage at the output swing. At this point, telescopic one-stage OTA is chosen as our design choice, with the gain-boosting topology in mind in case we need larger open-loop gain. However, after hand-analysis and repeated SPICE simulations, extra open-loop is not necessary and adding gain-boosting enhancement would be an over-design, add extra complexity and dissipate unnecessary power.

Close-loop gain of less than unity leads to the bigger feedback facto, $F$ and helps reduce the noise that is proportional to $1/F$. However, a large step needed at the input will create longer time for slewing. With all of these issues in mind, we begin designing our one-stage telescopic OTA.

II. Circuit Schematics and Parameters Tabulation

Here we have shown the final design of our complete schematics.

![Figure 2. Main amplifier schematic](image)

(I$I_1$, I$I_2$, and I$I_3$ will be generated by the bias network)
Figure 3. Biasing circuitry

Figure 4. CMFB circuit
Table 2: Final device sizes and parameters

<table>
<thead>
<tr>
<th>Device Type</th>
<th>W (um)</th>
<th>L (um)</th>
<th>gm (mS)</th>
<th>Id (mA)</th>
<th>Gm/Id (1/V)</th>
<th>Vov (V)</th>
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<tr>
<td>M1</td>
<td>500</td>
<td>0.35</td>
<td>20.4</td>
<td>1.2</td>
<td>17</td>
<td>0.118</td>
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<td>1.2</td>
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<td>0.118</td>
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<tr>
<td>M3</td>
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<td>1</td>
<td>16.7</td>
<td>1.2</td>
<td>13.92</td>
<td>0.144</td>
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<td>M4</td>
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<td>16.7</td>
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<td>9.17</td>
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<td>0.262</td>
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<td>500 (M=2)</td>
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<td>37</td>
<td>2.4</td>
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<tr>
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<td>0.27</td>
<td>0.015</td>
<td>18</td>
<td>0.111</td>
</tr>
<tr>
<td>Mc2</td>
<td>265</td>
<td>1</td>
<td>0.27</td>
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<td>Mc3</td>
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<td>0.29</td>
<td>0.015</td>
<td>19.33</td>
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<tr>
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<td>16.5</td>
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<td>0.29</td>
<td>0.015</td>
<td>19.33</td>
<td>0.103</td>
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<td>0.261</td>
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<td><strong>Main Bias</strong></td>
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<td>1.92</td>
<td>0.12</td>
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</table>

**Capacitor sizes**

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<tbody>
<tr>
<td>C_L</td>
<td>3pF</td>
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<tr>
<td>C_f</td>
<td>4pF</td>
</tr>
<tr>
<td>C_s</td>
<td>0.8pF</td>
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**Common-mode Voltages**

Vic = 0.8V (chosen such that MB1 that supplies tail-current has enough headroom)
Voc = 1.5V
III. Design Flow and Equations

We start with static accuracy requirement. Since we use one-stage telescopic approach which does not provide very high open-loop gain, we decide to allocate a large portion of total settling error (80%) to the static finite-gain error.

1) Static Accuracy

\[ \frac{1}{F} = 1 + c + \frac{C_i}{C_F}, \quad \frac{1}{F} > 1.2, \quad F := \frac{5}{7} \]

\[ \varepsilon_a := 0.08 \quad 80\% \text{ static error} \]

\[ a_{vo} := \frac{1}{F \cdot \varepsilon_a} \quad a_{vo} = 875 \]

Therefore, at \( V_{od_{\max}} \), the open-loop gain must be greater than 875 (see Fig. 5.1).

In order to further improve the open-loop gain by a factor of 2 or 3, we increased the channel lengths of the cascode devices to boost the output resistance. After the increase in the channel lengths and some SPICE simulations, the design achieves the desired minimum open-loop gain of 875 for reasonable \( V_{od} \) range. The maximum \( V_{od} \) that can satisfy \( a_{vo} > 875 \) would be ±1.8V.

2) Dynamic Range

full-scale output voltage range (peak to peak):

\[ \Delta V_{od} := 2(V_{DD} - 1.2V) \]

\[ P_{\text{sig}} := \frac{1}{2} \left( \frac{\Delta V_{od}}{2} \right)^2 \]

\[ n_f = 2\left(1 + \frac{V_{ov1}}{V_{ov3}} + \frac{V_{ov1}}{V_{ov9}}\right) \quad n_f := 2(1 + 0.5 + 0.5) \quad n_f = 4 \]

\[ P_{\text{noise}} = \frac{k_B T_r}{C_{\text{Eff}}} \frac{n_f}{F} \quad 10^{0.1 \cdot \text{DR}} = \frac{P_{\text{sig}}}{P_{\text{noise}}} \]

\[ C_{\text{Eff}} := 10^{0.1 \cdot \text{DR}} \frac{k_B T_r}{P_{\text{sig}}} \frac{n_f}{F} \quad C_{\text{Eff}} = 4.499\text{pF} \]

The next step is to satisfy the 85dB dynamic range requirement. We realize that output differential swing \( V_{od} \) must be high enough such that the need for huge load capacitors can be avoided. The output swing is in the order of \( V_{dd} - V_{dsat1} - V_{dsat3} - V_{dsat7} - V_{dsat9} - V_{dsat(mb1)} \) (see figure 2) or roughly \( V_{dd} - 5V_{dsat} \).

\( V_{ov} \) ratio (input to cascode) is picked to be 0.5 to minimize output noise. \( C_{\text{Eff}} \) includes load capacitor \( C_l \), \( C_F (1-F) \), and parasitic \( C_{db}, C_{sb}, C_{gd}, C_{gs} \) contributed from the transistors connecting to the differential output nodes. The value of \( C_F \) is chosen high enough such that the feedback factor \( F \) does not strongly depend on the input capacitor of the differential pair. Reducing the sampling and integrating capacitors helps increase the bandwidth of the OTA, but
results in a higher kT/C noise. We pick $C_L=3\,\text{pF}$, $C_F = 4\,\text{pF}$ and $C_s = 0.8\,\text{pF}$ such that $C_{\text{Leff}} = 3+4(1-0.7)+C_p \approx 4.5\,\text{pF}$ where $C_p$ notates the parasitic drain and source capacitances at the output nodes.

3) Settling Time (worst case)

$$V_{ov1} := 120\,\text{mV} \quad V_{\text{od\_step}} := 1\,\text{V}$$

$$\varepsilon_s := \varepsilon - \varepsilon_a \quad \varepsilon_s = 4 \times 10^{-4}$$

$$r := 0.63 \quad t_{\text{slew}} := r \cdot t_s \quad t_{\text{slew}} = 3.15\,\text{ns}$$

$$t_{\text{lin}} := t_s - t_{\text{slew}} \quad t_{\text{lin}} = 1.85 \times 10^{-9}\,\text{sec}$$

Slewing

$$t_{\text{slew}} = \frac{V_{\text{od\_step}} \cdot F}{F \cdot \text{SR}} - \frac{V_{ov1}}{F}$$

$$\text{SR} := \frac{V_{\text{od\_step}} \cdot F}{F \cdot t_{\text{slew}}} \quad \text{SR} = 0.569 \frac{V}{\text{ns}}$$

$$\frac{I_{ss}}{C_{\text{Leff}}} = I_{ss} := C_{\text{Leff}} \cdot \text{SR} \quad I_{ss} = 2.56\,\text{mA}$$

Settling

$$\varepsilon_{\text{lin}} := \varepsilon_s \cdot \frac{V_{\text{od\_step}} \cdot F}{V_{ov1}} \quad \varepsilon_{\text{lin}} = 2.381 \times 10^{-3}$$

$$n := -\ln(\varepsilon_{\text{lin}}) \quad n = 6.04$$

$$\tau := \frac{t_{\text{lin}}}{n} \quad \tau = 0.306\,\text{ns}$$

$$\tau = \frac{C_{\text{Leff}} \cdot 1}{g_{m1} \cdot F} \quad g_{m1} := \frac{C_{\text{Leff}} \cdot 1}{\tau \cdot F} \quad g_{m1} = 20.567\,\text{mS}$$

$$I_{D1} := \frac{g_{m1} \cdot V_{ov1}}{2} \quad I_{D1} = 1.234\,\text{mA}$$

$$\frac{I_{ss}}{I_{D1}} = 2.074$$

$$I_{ss} := \max(I_{ss}, 2 \cdot I_{D1}) \quad I_{ss} = 2.56\,\text{mA}$$

Finally we look at the settling time accuracy. We pick $V_{ov1}$ to be $0.12\,\text{V}$ in order for the transistor to stay in strong inversion while giving us good $g_{m}/I_D$ efficiency of 17. Further decreasing $V_{ov1}$ would be impractical and would lead transistors to operate in weak inversion. Also NMOS input pair is used for higher $g_{m}/I_D$ ratio. However, the disadvantages of using NMOS pair are body-effect that causes more mismatches, poor CMRR and higher input offset.
We then assign 63% of dynamic accuracy to slewing to achieve maximum power efficiency as shown in the calculation above.

We have about 55° phase margin for the differential loop gain but in practice, higher PM should be used. For the project, there is no layout consideration such as the use of multi-fingers to reduce the parasitic capacitances. However, in practice PM and frequency response would not be different after layout.

**Common-mode Feedback**

A simple single-ended common-mode feedback amplifier is used to bias our tail current source (See Fig.4 and 4.1). We make the CMFB loop-gain bandwidth to be comparable to half the differential loop-gain bandwidth (See the simulation result in figures 5.2.1, 5.2.2, 5.2.3 and 5.2.4). The polarity of the CMFB amplifier must be chosen correctly to ensure the negative feedback.

![Figure 4.1. Common-mode feedback loop](image)

To ensure that the common-mode feedback loop would not introduce instability into the system, we need to make sure that loop-gain bandwidth of the common-mode feedback loop $\omega_{u_{CMFB}} > 0.5 \omega_{u_{T}}$ where $\omega_{u_{T}}$ is the differential loop-gain bandwidth.

$$\omega_{u_{CMFB}} \geq \frac{C_{CMFB}}{C_{CMFB} + 0.5C_{in}} \cdot \frac{g_{mb1}}{g_{m1}} \cdot \frac{C_{L}}{C_{L}} \geq 0.5 \cdot \omega_{u_{T}} = 0.5 \cdot \frac{g_{m1}}{C_{L}}$$

Here $C_{in}$ denotes the capacitance at the input of the tail-current transistor $C_{mb1}$. Here we see that roughly $3C_{CMFB} = 0.5C_{in}$. We pick $C_{CMFB} = 80\text{fF}$. Again in practical bigger value should be used due to parasitic effects.

**Biasing network**

We need four current legs for four biases, three for the main amplifier and one for the CMFB circuit. We use high-swing cascode biasing network for $I_1$ and $I_2$ to supplement the biasing for the main amplifier’s high-impedence active PMOS cascode current load. Generating $I_3$ and $I_4$ however do not require high output impedance current sources. (See figure 3)
After we obtain these initial hand-analysis results, we enter the parameters into SPICE and figure out the device sizes and biasing network. The cascode pair is sized so that $V_{ov}$ ratio is 0.5 as mentioned earlier. The initial analysis gets us into 20-30% of specifications and more iteration is done to meet the specs with the goal of minimum power consumption. The next section summarizes all the specifications that our design met.

**IV. Verification and Simulation Results**

<table>
<thead>
<tr>
<th></th>
<th>Nominal</th>
<th>Slow</th>
<th>Fast</th>
<th>Spec</th>
<th>Figure</th>
</tr>
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<tr>
<td>Open loop gain (Vod=0V)</td>
<td>14100</td>
<td>14000</td>
<td>13800</td>
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<td></td>
</tr>
<tr>
<td>Open loop gain (Vod=1.8V)</td>
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<td>1150</td>
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<td>&gt; 875</td>
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<td>1100</td>
<td>914</td>
<td>&gt; 875</td>
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<td>Settling time, $t_b$ (Vod=1V) [ns]</td>
<td>4.81</td>
<td>4.89</td>
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<td>5.3.1, 5.3.3</td>
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<td>Settling time, $t_b$ (Vod=1.8V) [ns]</td>
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<td>Noise (Vod=0V) [$\mu$V-rms]</td>
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<td>Noise (Vod=1.8V) [$\mu$V-rms]</td>
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Table 3: Summary of OTA design performance

**Figure 5.1** DC Open-loop Gain $A_v$ vs. Vod (V)
Figure 5.2.1 Differential AC Loop Gain (dB) at Vod=0V

Figure 5.2.2 Differential AC Loop Gain (dB) at Vod=Vod_{\text{max}}=1.8V
Figure 5.2.3 Common-mode AC Loop Gain (dB) at $V_{od}=0V$

Figure 5.2.4 Common-mode AC Loop Gain (dB) at $V_{od}=V_{od_{max}}=1.8V$
Fig. 5.3.1 Step Response Voltage Transient ($V_{od}$ swings from 0V→1V)

Nominal
Slow
Fast

Fig. 5.3.2 Step Response Voltage Transient ($V_{od}$ swings 0.8V→1.8V)

Nominal
Slow
Fast
Figure 5.3.3  Step Response Voltage Transient (full scale)

Rise and fall time of the 5-V input step = 0.5ns as specified.
Fig. 5.3.3 Step Response Current Transient ($V_{od}$ swings from 0V → 1V)

Fig. 5.3.4 Step Response Current Transient ($V_{od}$ swings 0.8V → 1.8V)
Figure 5.4.1 Settling Error ($V_{od} \rightarrow 0V$)

Figure 5.4.2 Settling Error ($V_{od} \rightarrow 1.8V$)
Figure 5.5.1 Power Dissipation in main amplifier and biasing (Vod=0V)

Figure 5.5.2 Power Dissipation in main amplifier & biasing (Vod=1.8V)
Figure 5.6.1 Noise Spectrum (Vod = 0V)

Figure 5.6.2 Noise Spectrum (Vod = 1.8V)
V. Comments and Conclusion

In our design and HSPICE simulation, we proven the design specifications have met. However we have assumed one-finger very large devices for each transistor. But in practice, there will be multiple fingers consideration for more area-efficiency. We have added well-to-substrate reversed-bias diode in the cascode to give us more realistic noise and transient simulations. Due to the fact that we do not use multi-fingers transistors for our simulation, the practical parasitics cannot be simulated. Some parasitic effects are not accounted for because they will contribute little effect on the results. For instance, the extra parasitic capacitors in bias circuits will slightly degrade the phase margin of the bias circuit but they act like bypass capacitance in the frequencies of interest. Some other parasitic capacitors are either tied to Vdd or Vss or ground and contribute no effect. However, the drain, source, gate and body parasitics are included and correctly simulated.

For the biasing network, we use 10:1 current ratio between transistors which is practical and any bigger ratio will cause significant mismatches. After all, all the specifications are met over all process corners while the main amplifier consumes 7.2mW of power and the bias circuits consumes 1.9mW.
**APPENDIX 1: DESIGN SPICE DECK**

**********EE240 Project************

VDD VDD 0 3V
VDD_B VDD_B 0 3V
IREF VDD_B BIAS1 120u

VID VID 0 DC 0 AC 1 PULSE (0 5 0 .5n .5n 5n 100N)
VIC VIC 0 DC .8V

XIN VID VIC Vi+ Vi- BALUN
XIN2 VD VIC Vx+ Vx- BALUN
XIN3 VD VIC Vy+ Vy- BALUN

.PARAM W1=500UM L1=.35UM +
+ W3=800UM L3=1u
+ W7=800uM L7=1u
+ wbn=35u lbn=.35u
+ wbp=80u lbp=1u
+ w9=800uM 19u

**Tail current source***

mb1 vx cmfb_out 0 0 nmos w=w1 l=l1 m=2

***CFMB AMP***

mc1 dcl cmfb vxx vxx pmos w=w7 l=17 m=.33
mc2 cmfb_out vcm vxx vxx pmos w=w7 l=17 m=.33
mc3 cmfb_out dcl 0 0 nmos w=w1 l=l1 m=0.33
mc4 dcl dcl 0 0 nmos w=w1 l=l1 m=033
rrr vdd_b vcm 100t
rr2 vcm 0 100t
crr vdd_b vcm 500f
cr2 vcm 0 500f
cc cmfb 0 4p

***Input transistors***

M1 d1 VX+ VX 0 NMOS w=W1 L=L1 m=1
M2 d2 VX- VX 0 NMOS w=W1 L=L1 m=1

***NMOS CASCODE***

M3 Vo+ b1 d2 0 NMOS W=W3 L=L3 m=1
M4 Vo- b1 d1 0 NMOS W=W3 L=L3 m=1

***PMOS CURRENT SOURCE***

M7 D7 VB5 VDD VDD PMOS W=W7 L=L7 M=1
M8 D8 VB5 VDD VDD PMOS W=W7 L=L7 M=1
M9 Vo+ VB6 D7 D7 PMOS W=W9 L=19 M=1
M10 Vo- VB6 D8 D8 PMOS W=W9 L=19 M=1

***PMOS CASCODE WELL DIODES***

d9 0 d7 dwell a='(w9*13u)' d10 0 d8 dwell a='(w9*13u)'

***HIGH SWING PMOS BIAS***

MB5 VB7 VB5 VDD_B VDD_B PMOS W=Wbp L=Lbp M=1
MB6 VB5 VB6 VB7 VB7 PMOS W=Wbp L=Lbp M=1
MB7 VB8 VB6 VDD_B VDD_B PMOS W=Wbp L=Lbp M=.25
MB8 VB6 VB6 VB8 VB8 PMOS W=Wbp L=Lbp M=1

***MAIN BIAS***

Mbias1 bias1 bias1 bias2 0 NMOS W=Wbn L=Lbn m=1
Mbias2 bias2 bias2 0 0 NMOS W=Wbn L=Lbn m=1
Mbias3 bias3 bias1 bias4 0 NMOS W=Wbn L=Lbn m=1
Mbias4 bias4 bias2 0 0 NMOS W=Wbn L=Lbn m=1
Mbias5 bias3 bias3 VDD_B VDD_B PMOS W=Wbp L=Lbp m=1

***M3 AND M4 BIAS***

Mbias6 b1 bias3 VDD_B VDD_b PMOS W=Wbp L=Lbp m=1
Mbias7 b1 b1 0 0 nmos W=3.75u L=1u m=1

***M7-9 BIAS***

Mbias8 vb6 bias1 bias5 0 NMOS W=Wbn L=Lbn m=1
Mbias9 bias5 bias2 0 0 NMOS W=Wbn L=Lbn m=1
Mbias10 vb5 bias1 bias6 0 NMOS W=Wbn L=Lbn m=1
Mbias11 bias6 bias2 0 0 NMOS W=Wbn L=Lbn m=1

***CMFB AMP BIAS***

Mbias12 vxx bias3 VDD_b VDD_B PMOS W=Wbp L=Lbp m=.25

***FEEDBACK***

CF1 VO+ Vy- 4p
CF2 VO- Vy+ 4p
CS1 Vy+ VI+ .8p
CS2 Vy- VI- .8p
RF1 VO+ Vy- 10t
RF2 VO- Vy+ 10t
RS1 Vy+ VI+ 50t
RS2 Vy- VI- 50t

***CMFB***

CCMF1 VO+ cmfb 80f
CCMF2 VO- cmfb 80f
RCMF1 VO+ cmfb 10T
RCMF2 VO- cmfb 10T

CL+ VO+ 0 3pF
CL- VO- 0 3pF
XOUT VOD VOC VO+ VO- BALUN

.include 'util.inc'

.noise v(vod) vid
/*.dc vid -3m 3m .01m
.TRAN .01N 10N
.ac dec 10 1u 10t
*.probe vdb(tv) p(tv) vdb(ti)
*.tf v(vod) vid
.model dwell d c30=1e-4 is=1e-5 m=0.5
 hv=40
.op
.options dccap post=2 brief
.lib 'cmos35.txt' nominal
.alter slow
.lib 'cmos35.txt' slow
.alter fast
.lib 'cmos35.txt' fast
.end