A Fast-Settling, High Dynamic Range Fully Differential Operational Transconductance Amplifier

Eddie Ng eddieng@eecs.berkeley.edu

Kenneth Oo kenoo@eecs.berkeley.edu

== EE240 Class Project, Spring 2002 ==
Professor B.E. Boser
University of California, Berkeley

Abstract

In this project, we have designed a fully-differential operational transconductance amplifier with capacitive feedback network producing a close-loop gain of 0.2. The OTA was designed in the single-stage telescopic topology and simulation with HSPICE and achieved a very fast settling time of less than 5ns and a settling accuracy of at least 0.2%. The OTA has the differential output swing of ±1.8V and a dynamic range greater than 85dB while consuming 7.2mW from a 3V supply for the main amplifier and 1.9mW for the bias network.

I. Design Approach and Decisions

Choosing the right overall circuit topology for a given set of specifications so as to avoid over-designing the circuit is one of the most critical design decisions to start out with. We begin investigating the specifications of the project very closely, and look at the pool of candidates for the best circuit topology. For the single-stage design, we consider telescopic, folded-cascode and gain-boosting amplifiers. Two-stage design consists of using a full 2-stage or a preamp followed by a full-stage amplifier. However, the fact that we only need 0.2% settling accuracy tells us that the open-loop gain for the OTA need not be extremely high (as shown later in Section III). In fact, an open-loop gain of more or less 1000 at around the maximum differential swing should suffice. Hence, to employ the design in a two-stage or gain-boosting topology may give excessive dc gain while dissipate much more power.

Supply V_{DD}	3V
Closed-loop gain, c	0.2
DR at output	≥ 85 dB
Settling accuracy	≤ 0.2%
Settling time, t_s	≤ 5 ns
Process	EE240 0.35um
Process corners	slow/nominal/fast

Table 1: Project specifications

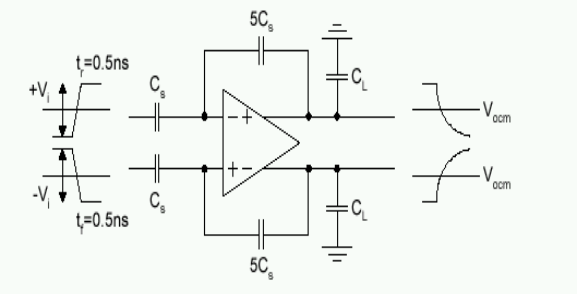


Figure 1 Conceptual diagram of amplifier configured as gain stage.

Dynamic range of 85dB indicates that the OTA should be designed with large output swing range and that the integrator will need a large load capacitor at the output. A full two-stage design is the best candidate in terms of the output differential range, but the major drawback is the need for a minimum of four current legs (all drawing comparable currents) and thus may have big impact on the power consumption. At this point we decided to forego the 2-stage design.

In addition, a 5ns settling time is quite a stringent requirement and this makes the fast and simple single-stage telescopic or folded-cascode very attractive. The folded-cascode design suffers from the extra current leg introduced by the folded structure while only providing one extra V_{ds}^{sat} headroom advantage at the output swing. At this point, telescopic one-stage OTA is chosen as our design choice, with the gain-boosting topology in mind in case we need larger open-loop gain. However, after hand-analysis and repeated SPICE simulations, extra open-loop is not necessary and adding gain-boosting enhancement would be an over-design, add extra complexity and dissipate unnecessary power.

Close-loop gain of less than unity leads to the bigger feedback facto, F and helps reduce the noise that is proportional to 1/F. However, a large step needed at the input will create longer time for slewing. With all of these issues in mind, we begin designing our one-stage telescopic OTA.

II. Circuit Schematics and Parameters Tabulation

Here we have shown the final design of our complete schematics.

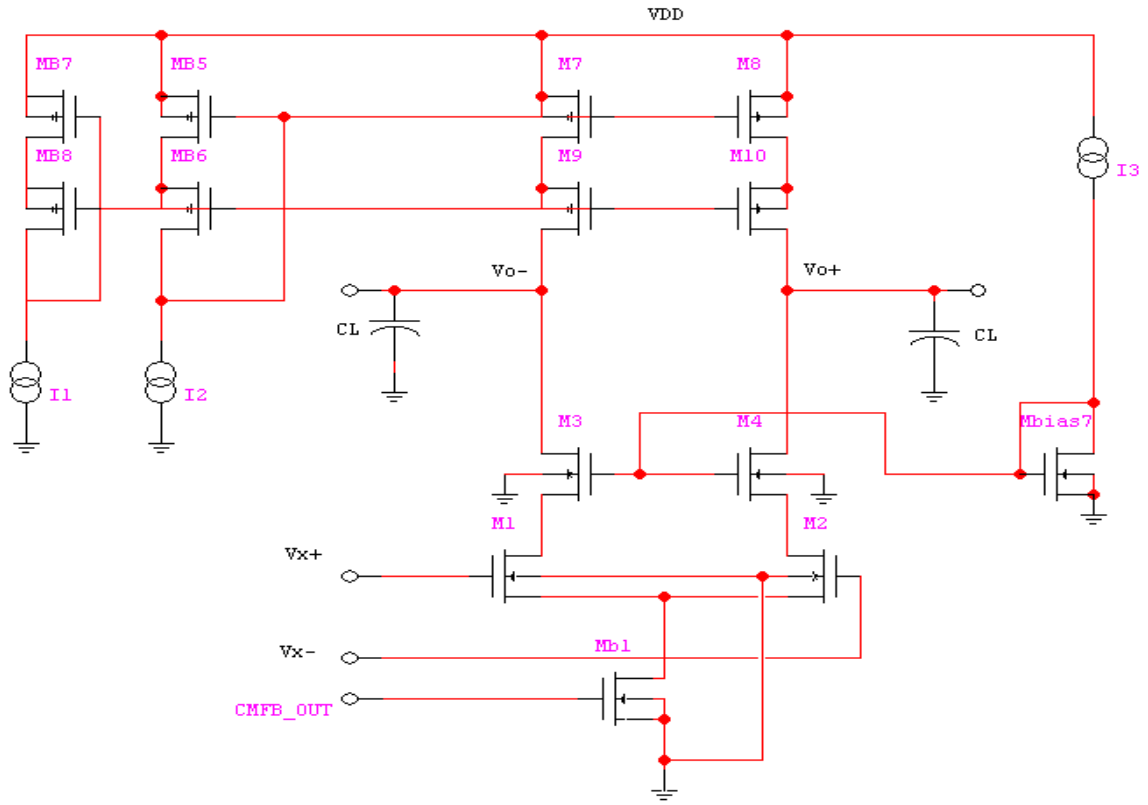


Figure 2. Main amplifier schematic (I_1, I_2, and I_3 will be generated by the bias network)

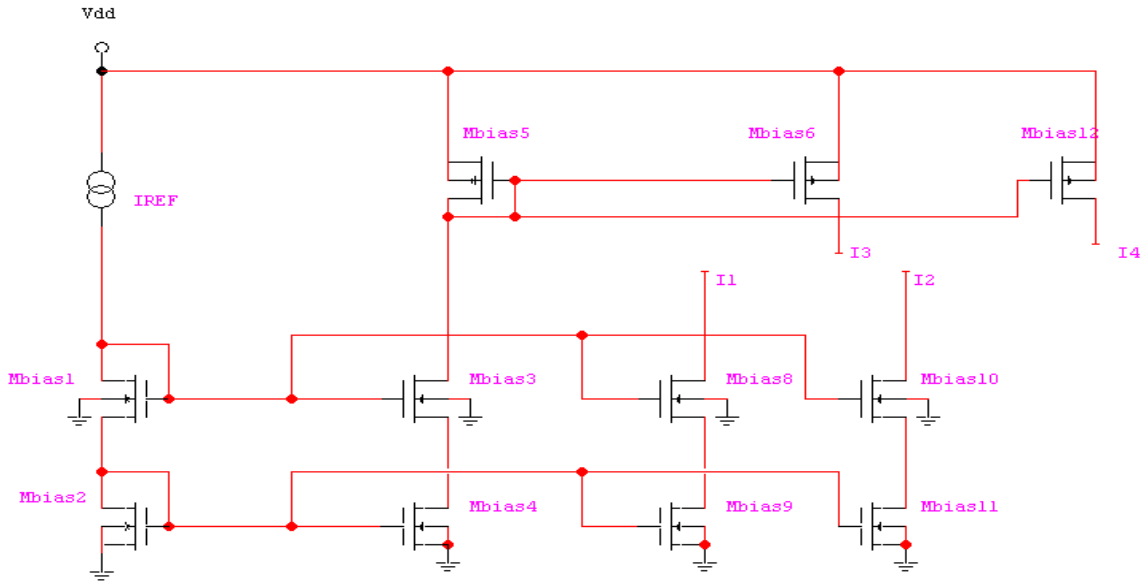


Figure 3. Biasing circuitry

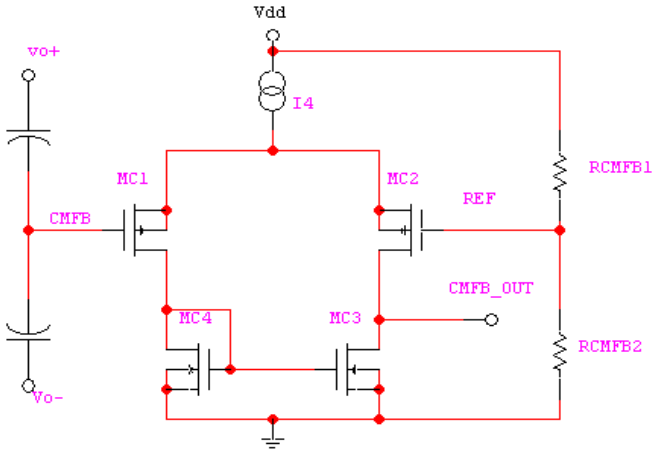


Figure 4. CMFB circuit

Table 2: Final device sizes and parameters

	W (um)	L (um)	gm (mS)	Id (mA)	Gm/Id (1/V)	Vov (V)
Main Amplifier						
M1	500	0.35	20.4	1.2	17	0.118
M2	500	0.35	20.4	1.2	17	0.118
M3	800	1	16.7	1.2	13.92	0.144
M4	800	1	16.7	1.2	13.92	0.144
M7	800	1	9.17	1.2	7.64	0.262
M8	800	1	9.17	1.2	7.64	0.262
M9	800	1	9.6	1.2	8	0.25
M10	800	1	9.6	1.2	8	0.25
CMFB Amplifier						
Mb1	500 (M=2)	0.35	37	2.4	15.42	0.130
Mc1	265	1	0.27	0.015	18	0.111
Mc2	265	1	0.27	0.015	18	0.111
Mc3	16.5	0.35	0.29	0.015	19.33	0.103
Mc4	16.5	0.35	0.29	0.015	19.33	0.103
PMOS Cascode Bias						
Mb5	80	1	0.92	0.12	7.67	0.261
Mb6	80	1	0.92	0.12	7.67	0.261
Mb7	20	1	0.31	0.12	2.58	0.774
Mb8	80	1	0.92	0.12	7.67	0.261
Main Bias						
Mbias1	35	0.35	1.92	0.12	16	0.125
Mbias2	35	0.35	1.92	0.12	16	0.125
Mbias3	35	0.35	1.92	0.12	16	0.125
Mbias4	35	0.35	1.92	0.12	16	0.125
Mbias5	80	1	0.98	0.12	8.17	0.245
Mbias6	80	1	0.98	0.12	8.17	0.245
Mbias7	3.75	1	0.34	0.12	2.83	0.706
Mbias8	3	0.35	1.9	0.12	15.83	0.126
Mbias9	3	0.35	1.9	0.12	15.83	0.126
Mbias10	3	0.35	1.9	0.12	15.83	0.126
Mbias11	3	0.35	1.9	0.12	15.83	0.126
Mbias12	20	1	0.24	0.03	8	0.25

Capacitor sizes

C_L	3pF
C_f	4pF
C_s	0.8pF

Common-mode Voltages

Vic = 0.8V (chosen such that MB1 that supplies tail-current has enough headroom)
Voc = 1.5V

III. Design Flow and Equations

We start with static accuracy requirement. Since we use one-stage telescopic approach which does not provide very high open-loop gain, we decide to allocate a large portion of total settling error (80%) to the static finite-gain error.

1) Static Accuracy

$\frac{1}{F} = 1 + c + \frac{C_i}{C_f}$ $\frac{1}{F} > 1.2$ $F := \frac{5}{7}$

$\varepsilon_a := .8 \cdot \varepsilon$ 80% static error $\varepsilon_a = 1.6 \times 10^{-3}$

$a_{vo} := \frac{1}{F \cdot \varepsilon_a}$ $a_{vo} = 875$

Therefore, at Vod_{max}, the open-loop gain must be greater than 875 (see Fig. 5.1).
In order to further improve the open-loop gain by a factor of 2 or 3, we increased the channel lengths of the cascode devices to boost the output resistance. After the increase in the channel lengths and some SPICE simulations, the design achieves the desired minimum open-loop gain of 875 for reasonable V_{od} range. The maximum V_{od} that can satisfy $a_{vo} > 875$ would be ±1.8V.

2) Dynamic Range

full-scale output voltage range (peak to peak): $\Delta V_{od} := 2 \cdot (V_{DD} - 1.2V)$

$P_{sig} := \frac{1}{2} \cdot \left(\frac{\Delta V_{od}}{2} \right)^2$

$n_f = 2\left(1 + \frac{Vov1}{Vov3} + \frac{Vov1}{Vov9}\right)$ $n_f := 2 \cdot (1 + 0.5 + 0.5)$ $n_f = 4$

$P_{noise} = \frac{k_B \cdot T_r}{C_{Leff}} \cdot \frac{n_f}{F}$ $10^{0.1 \cdot DR} = \frac{P_{sig}}{P_{noise}}$

$C_{Leff} := 10^{0.1 \cdot DR} \cdot \frac{k_B \cdot T_r \cdot \frac{n_f}{F}}{P_{sig}}$ $C_{Leff} = 4.499pF$

The next step is to satisfy the 85dB dynamic range requirement. We realize that output differential swing Vod must be high enough such that the need for huge load capacitors can be avoided. The output swing is in the order of $V_{dd} - V_{dsat1} - V_{dsat3} - V_{dsat7} - V_{dsat9} - V_{dsat(mb1)}$ (see figure 2) or roughly $V_{dd} - 5V_{dsat}$.

V_{ov} ratio (input to cascode) is picked to be 0.5 to minimize output noise. C_{Leff} includes load capacitor C_L, C_F (1-F), and parasitic C_{db}, C_{sb}, C_{gd}, C_{gs} contributed from the transistors connecting to the differential output nodes. The value of C_F is chosen high enough such that the feedback factor F does not strongly depend on the input capacitor of the differential pair. Reducing the sampling and integrating capacitors helps increase the bandwidth of the OTA, but

results in a higher kT/C noise. We pick C_L=3pF, C_F = 4pF and C_s = 0.8pF such that C_{Leff} = 3+4(1-0.7)+C_p = ~ 4.5pF where C_p notates the parasitic drain and source capacitances at the output nodes.

3) Settling Time (worst case)

$V_{ov1} := 120mV$ $V_{od\_step} := 1V$

$\varepsilon_s := \varepsilon - \varepsilon_a$ $\varepsilon_s = 4 \times 10^{-4}$

$r := 0.63$ $t_{slew} := r \cdot t_s$ $t_{slew} = 3.15ns$

$t_{lin} := t_s - t_{slew}$ $t_{lin} = 1.85 \times 10^{-9}\ sec$

Slewing

$$t_{slew} = \frac{\frac{V_{od\_step}}{F} - V_{ov1}}{F \cdot SR} \qquad SR := \frac{\frac{V_{od\_step}}{F} - V_{ov1}}{F \cdot t_{slew}} \qquad SR = 0.569\frac{V}{ns}$$

$$SR = \frac{I_{ss}}{C_{Leff}} \qquad I_{ss} := C_{Leff} \cdot SR \qquad I_{ss} = 2.56mA$$

Settling

$$\varepsilon_{lin} := \varepsilon_s \cdot \frac{V_{od\_step} \cdot F}{V_{ov1}} \qquad \varepsilon_{lin} = 2.381 \times 10^{-3}$$

$n := -\ln(\varepsilon_{lin})$ $n = 6.04$

$$\tau := \frac{t_{lin}}{n} \qquad \tau = 0.306ns$$

$$\tau = \frac{C_{Leff}}{g_{m1}} \cdot \frac{1}{F} \qquad g_{m1} := \frac{C_{Leff}}{\tau} \cdot \frac{1}{F} \qquad g_{m1} = 20.567mS$$

$$I_{D1} := g_{m1} \cdot \frac{V_{ov1}}{2} \qquad I_{D1} = 1.234mA$$

$$\frac{I_{ss}}{I_{D1}} = 2.074$$

$I_{ss} := \max(I_{ss}, 2 \cdot I_{D1})$ $I_{ss} = 2.56mA$

Finally we look at the settling time accuracy. We pick V_{ov1} to be 0.12V in order for the transistor to stay in strong inversion while giving us good g_m/I_D efficiency of 17. Further decreasing V_{ov1} would be impractical and would lead transistors to operate in weak inversion. Also NMOS input pair is used for higher g_m/I_D ratio. However, the disadvantages of using NMOS pair are body-effect that causes more mismatches, poor CMRR and higher input offset.

We then assign 63% of dynamic accuracy to slewing to achieve maximum power efficiency as shown in the calculation above.

We have about 55^0 phase margin for the differential loop gain but in practice, higher PM should be used. For the project, there is no layout consideration such as the use of multi-fingers to reduce the parasitic capacitances. However, in practice PM and frequency response would not be different after layout.

Common-mode Feedback

A simple single-ended common-mode feedback amplifier is used to bias our tail current source (See Fig.4 and 4.1). We make the CMFB loop-gain bandwidth to be comparable to half the differential loop-gain bandwidth (See the simulation result in figures 5.2.1, 5.2.2, 5.2.3 and 5.2.4). The polarity of the CMFB amplifier must be chosen correctly to ensure the negative feedback.

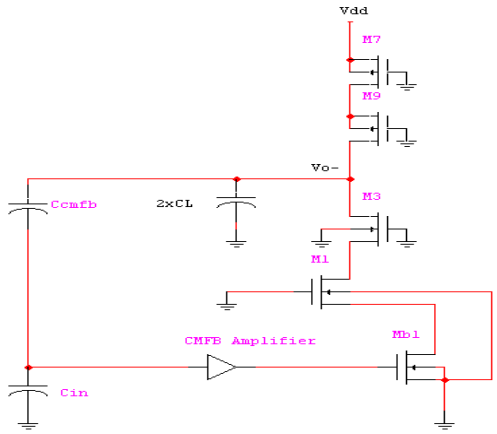


Figure 4.1. Common-mode feedback loop

To ensure that the common-mode feedback loop would not introduce instability into the system, we need to make sure that loop-gain bandwidth of the common-mode feedback loop $\omega_{u\_CMFB} > 0.5\omega_{u\_T}$ where ω_{u_T} is the differential loop-gain bandwidth.

$$\omega_{u\_CMFB} \approx \frac{C_{CMFB}}{C_{CMFB} + 0.5C_{in}} \cdot \frac{g_{mb1}}{C_L} \geq 0.5 \cdot \omega_{u\_T} = 0.5 \cdot \frac{g_{m1}}{C_L}$$

Here C_{in} denotes the capacitance at the input of the tail-current transistor C_{Mb1}. Here we see that roughly $3C_{CMFB} = 0.5C_{in}$. We pick C_{CMFB} = 80fF. Again in practical bigger value should be used due to parasitic effects.

Biasing network

We need four current legs for four biases, three for the main amplifier and one for the CMFB circuit. We use high-swing cascode biasing network for I_1 and I_2 to supplement the biasing for the main amplifier's high-impedence active PMOS cascode current load. Generating I_3 and I_4 however do not require high output impedance current sources. (See figure 3)

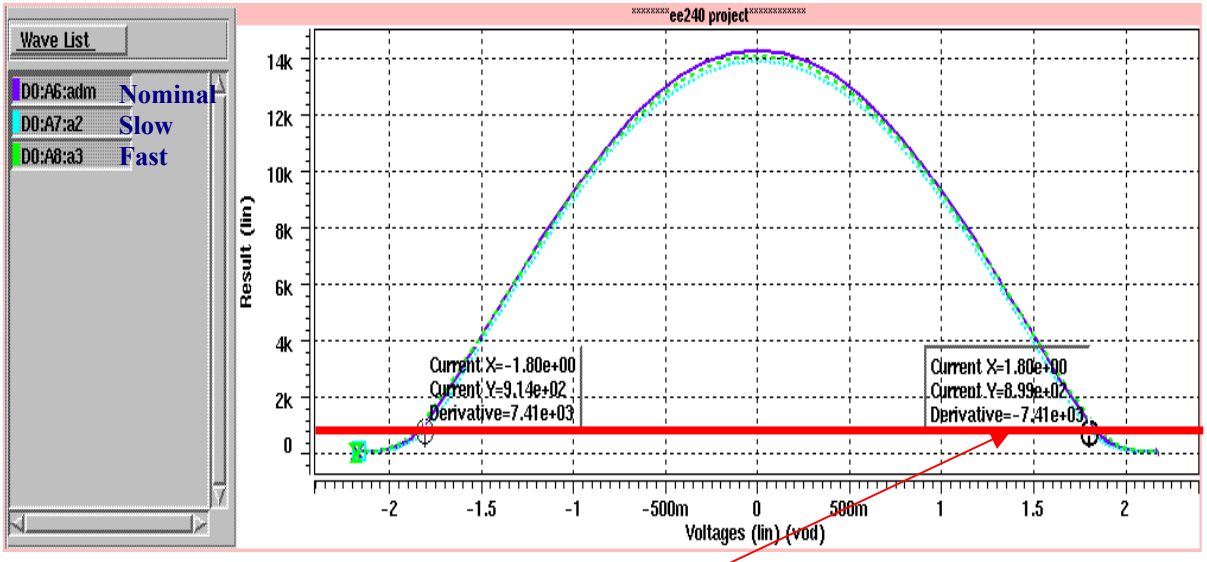
After we obtain these initial hand-analysis results, we enter the parameters into SPICE and figure out the device sizes and biasing network. The cascode pair is sized so that V_{ov} ratio is 0.5 as mentioned earlier. The initial analysis gets us into 20-30% of specifications and more iteration is done to meet the specs with the goal of minimum power consumption. The next section summarizes all the specifications that our design met.

IV. Verification and Simulation Results

	Nominal	Slow	Fast	Spec	Figure
Open loop gain (Vod=0V)	14100	14000	13800		
Open loop gain (Vod=1.8V)	1050	1150	900	> 875	5.1
Open loop gain (Vod=-1.8V)	1000	1100	914	> 875	5.1
Settling time, t_s (Vod=1V) [ns]	4.81	4.89	4.93	< 5.0	5.3.1, 5.3.3
Settling time, t_s (Vod=1.8V) [ns]	4.9	4.62	4.965	< 5.0	5.3.2, 5.3.4
Phase margin (Vod=0V)	55.8	55	56		5.2.1
Phase margin (Vod=1.8V)	57.2	56.2	56.8		5.2.2
Noise (Vod=0V) [μV-rms]	71.03	71.55	70.51	< 71.57	5.6.1
Noise (Vod=1.8V) [μV-rms]	70.97	71.54	70.54	< 71.57	5.6.2
DR [dB]	85.073654	85.00417	85.12644	> 85	
Power Dissipation (Main Amplifier)	7.2	7.2	7.2		5.5.1
Power Dissipation (Bias Circuit)	1.95	1.95	1.95		5.5.2
DM Loop unity gain frequency ($f_{u\text{-}T}$)	364MHz	364MHz	364MHz		5.2.1, 5.2.2
CM loop unity gain frequency ($f_{u\text{-}CMFB}$)	185MHz	185MHz	185MHz		5.2.3, 5.2.4

Table 3: Summary of OTA design performance

Figure 5.1 DC Open-loop Gain Av_o vs. Vod (V)



Minimum Avo: 875

Figure 5.2.1 Differential AC Loop Gain (dB) at Vod=0V

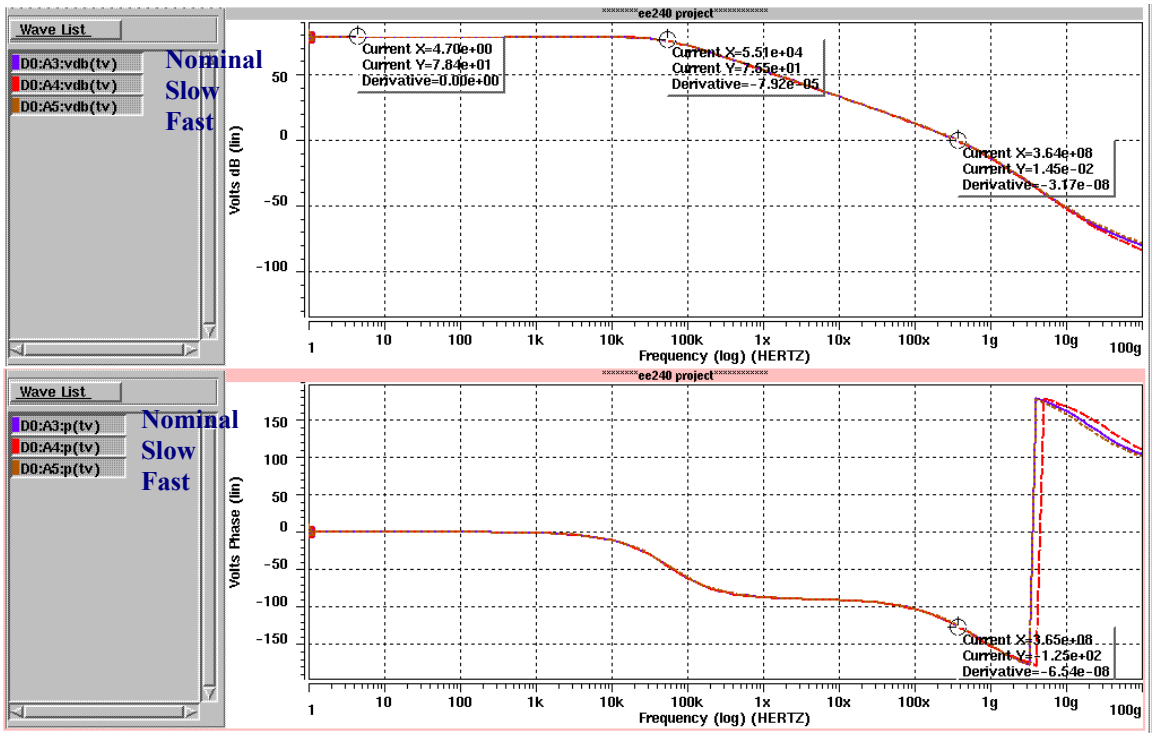


Figure 5.2.2 Differential AC Loop Gain (dB) at Vod=Vod_{max}=1.8V

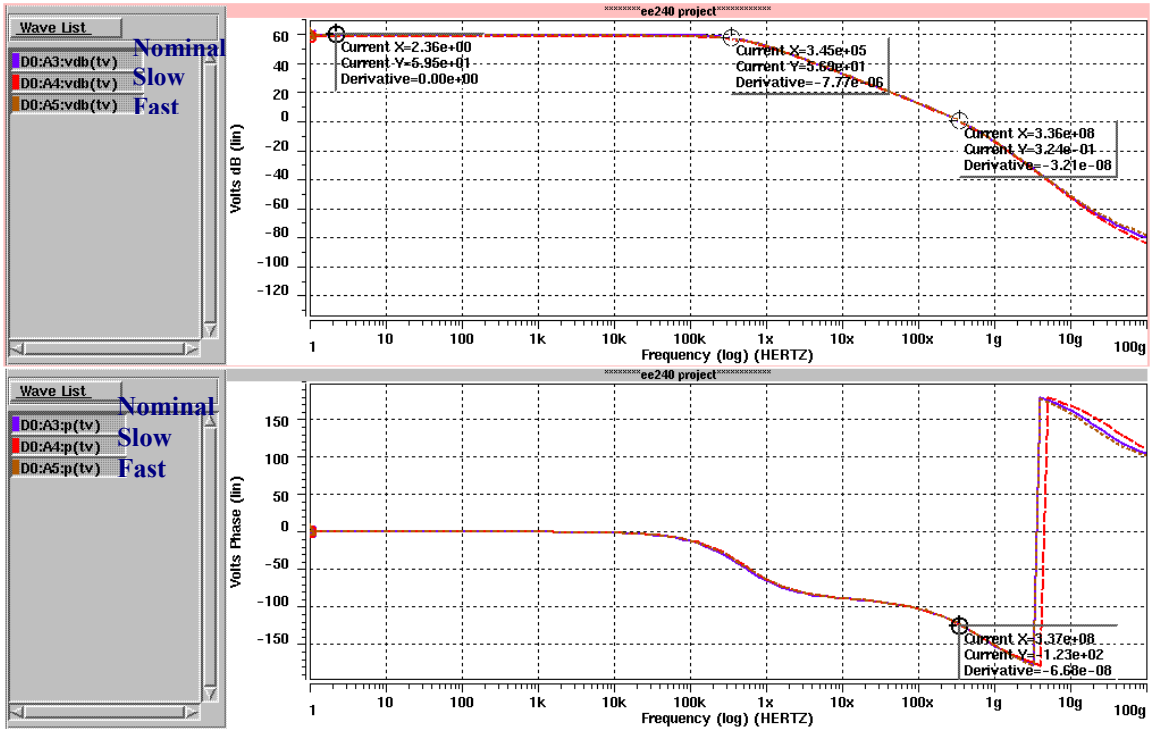


Figure 5.2.3 Common-mode AC Loop Gain (dB) at Vod=0V

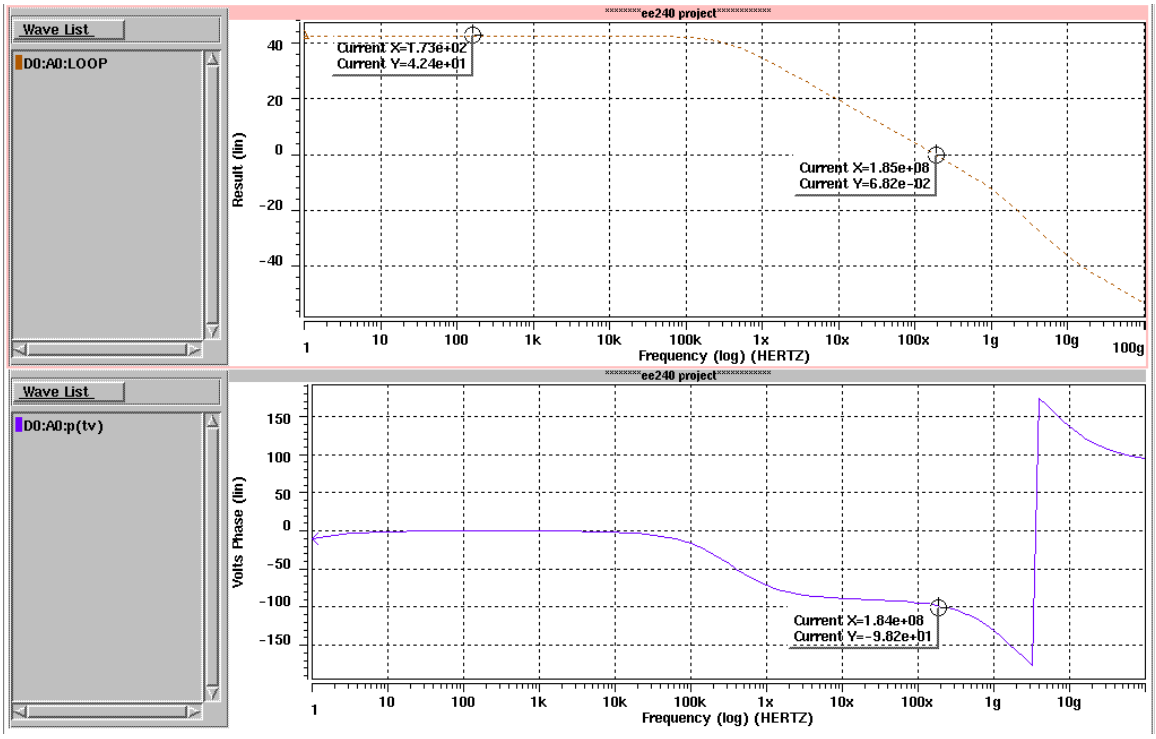


Figure 5.2.4 Common-mode AC Loop Gain (dB) at Vod=Vod_{max}=1.8V

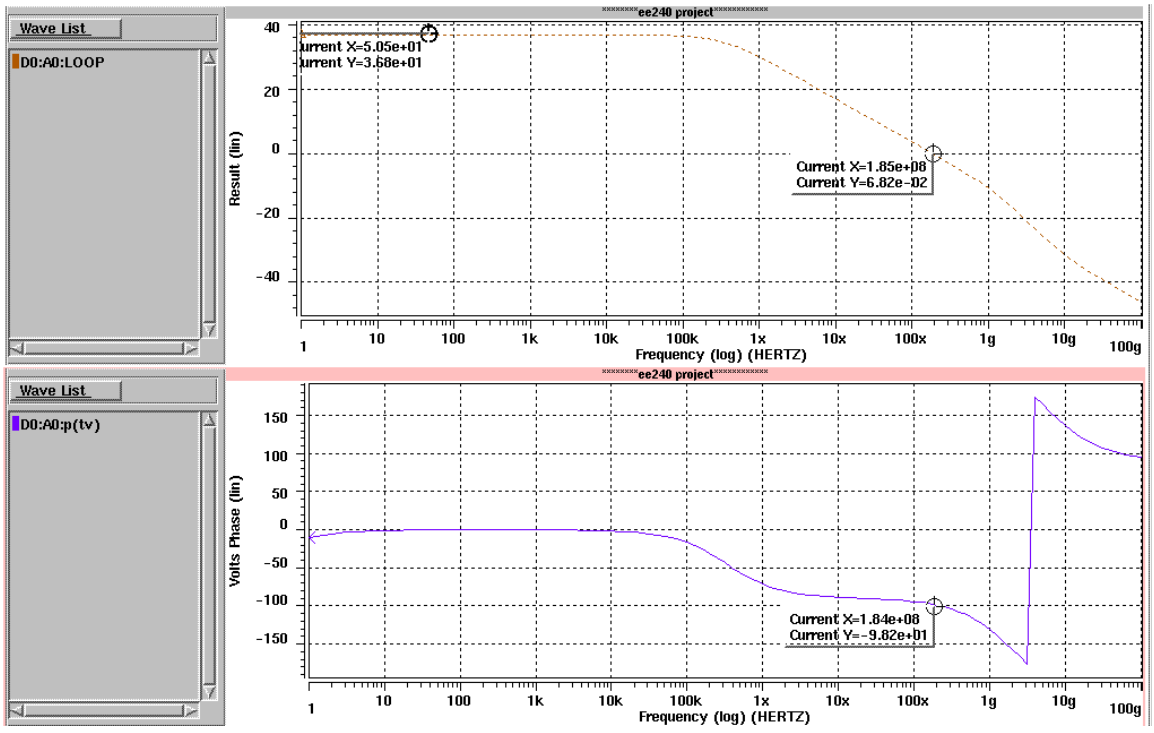


Fig. 5.3.1 Step Response Voltage Transient (V_{od} swings from 0V→1V)

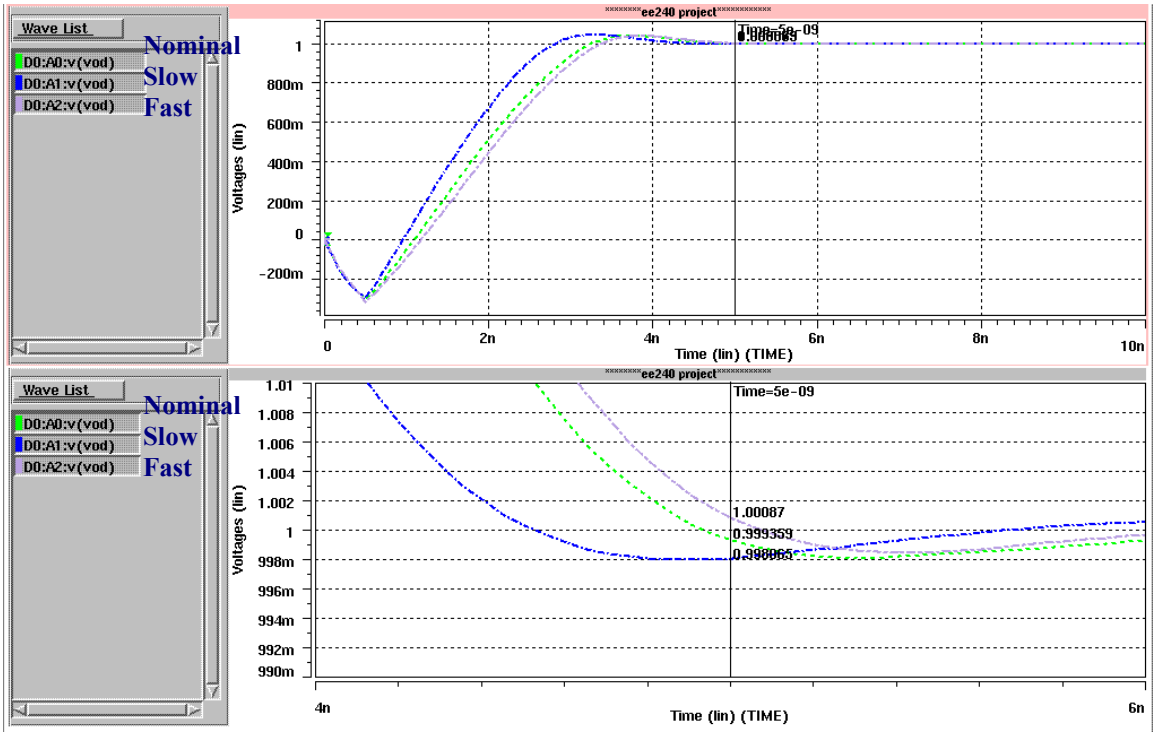


Fig. 5.3.2 Step Response Voltage Transient (V_{od} swings 0.8V→1.8V)

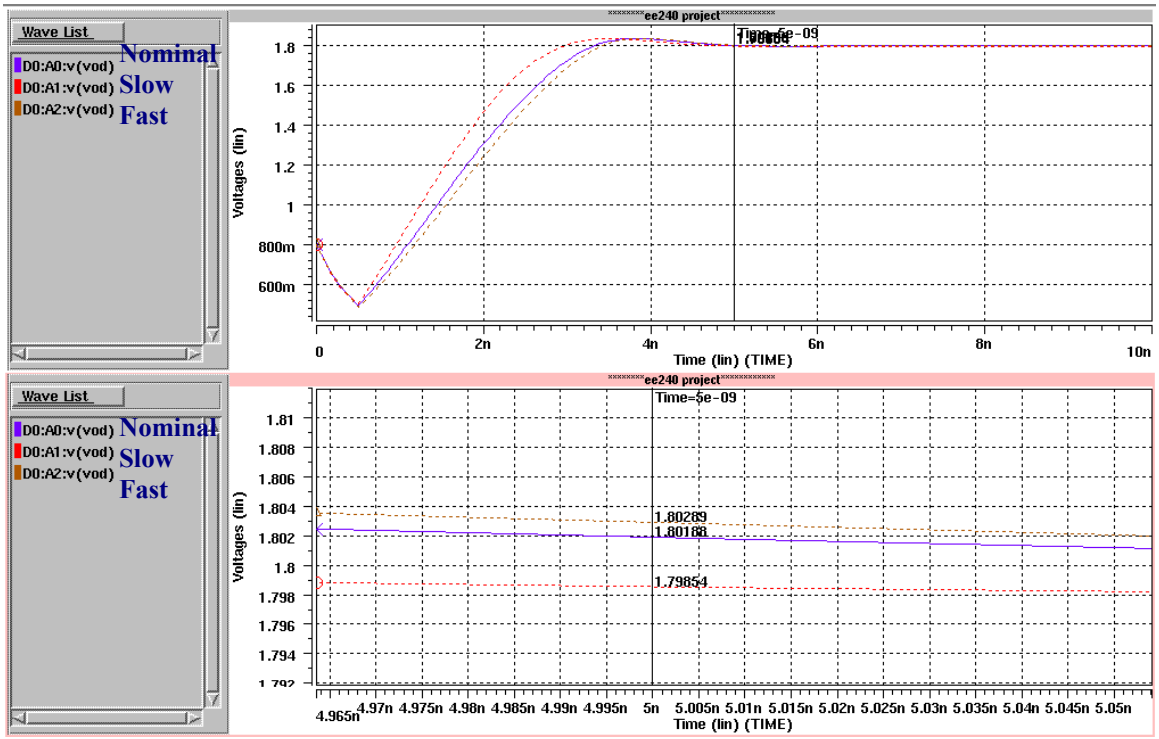
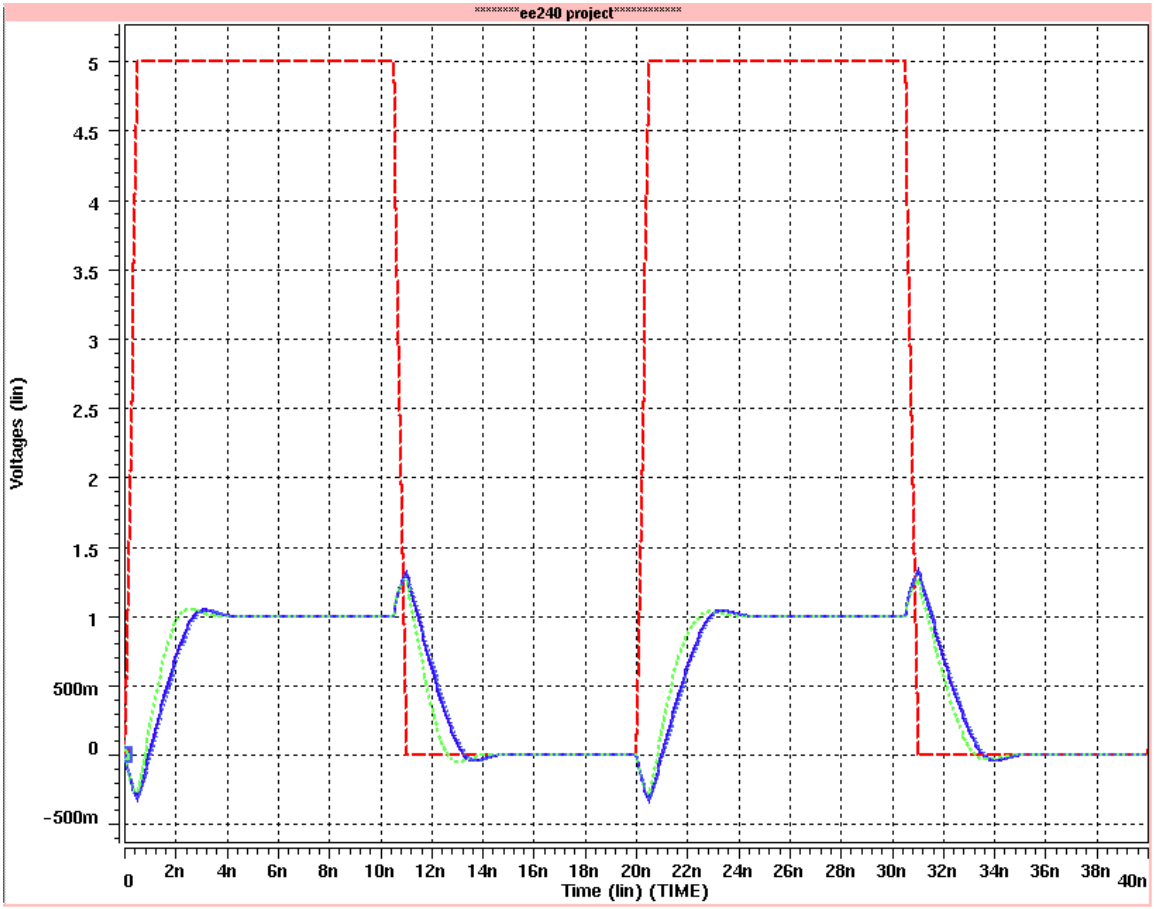


Figure 5.3.3 Step Response Voltage Transient (full scale)



Rise and fall time of the 5-V input step = 0.5ns as specified.

Fig. 5.3.3 Step Response Current Transient (V_{od} swings from 0V→1V)

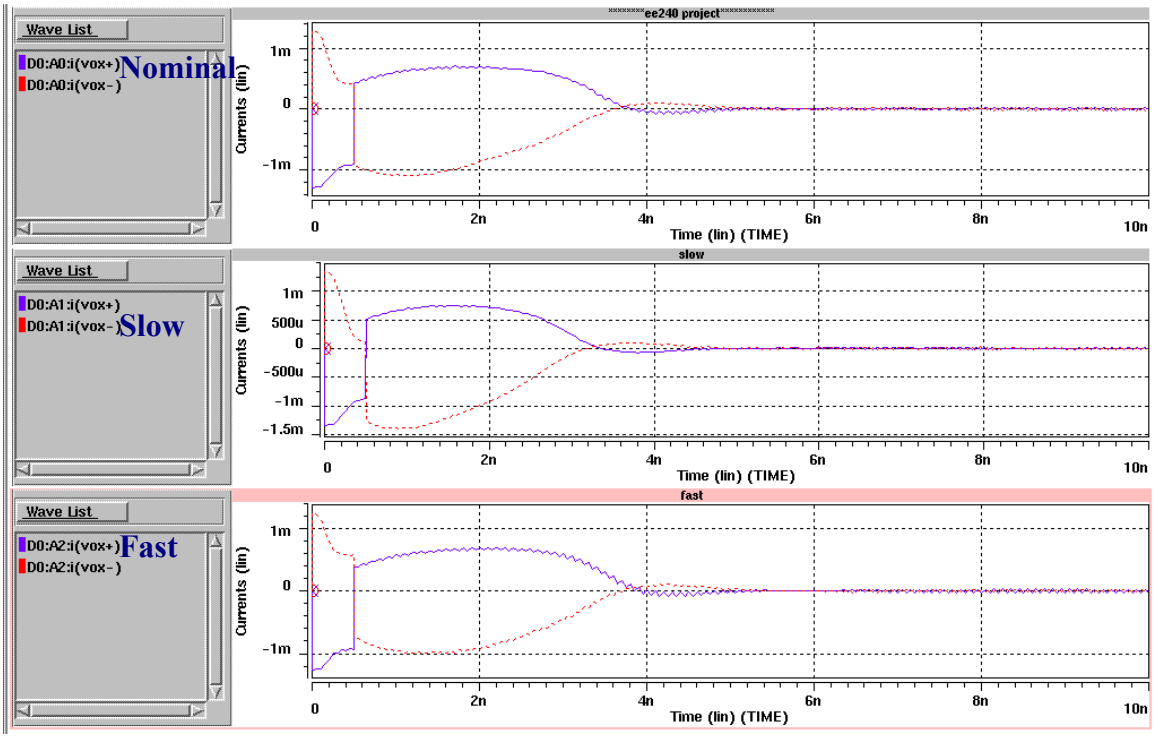


Fig. 5.3.4 Step Response Current Transient (V_{od} swings 0.8V→1.8V)

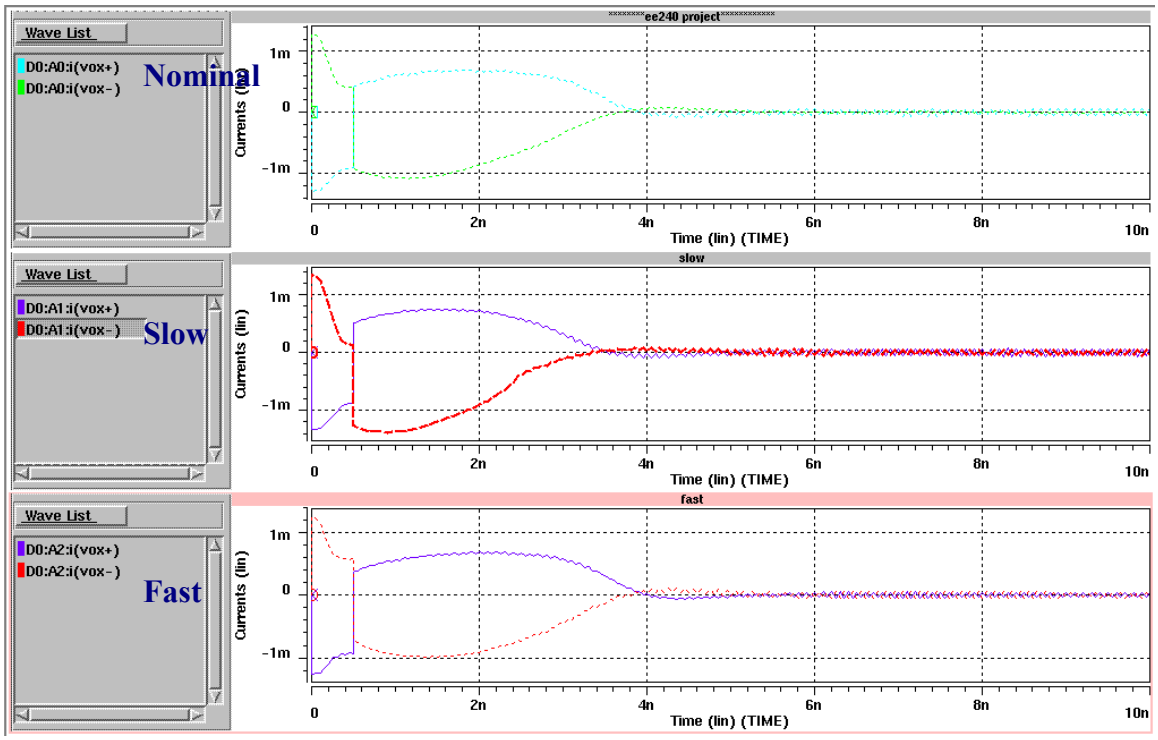


Figure 5.4.1 Settling Error ($V_{od} \rightarrow 0V$)

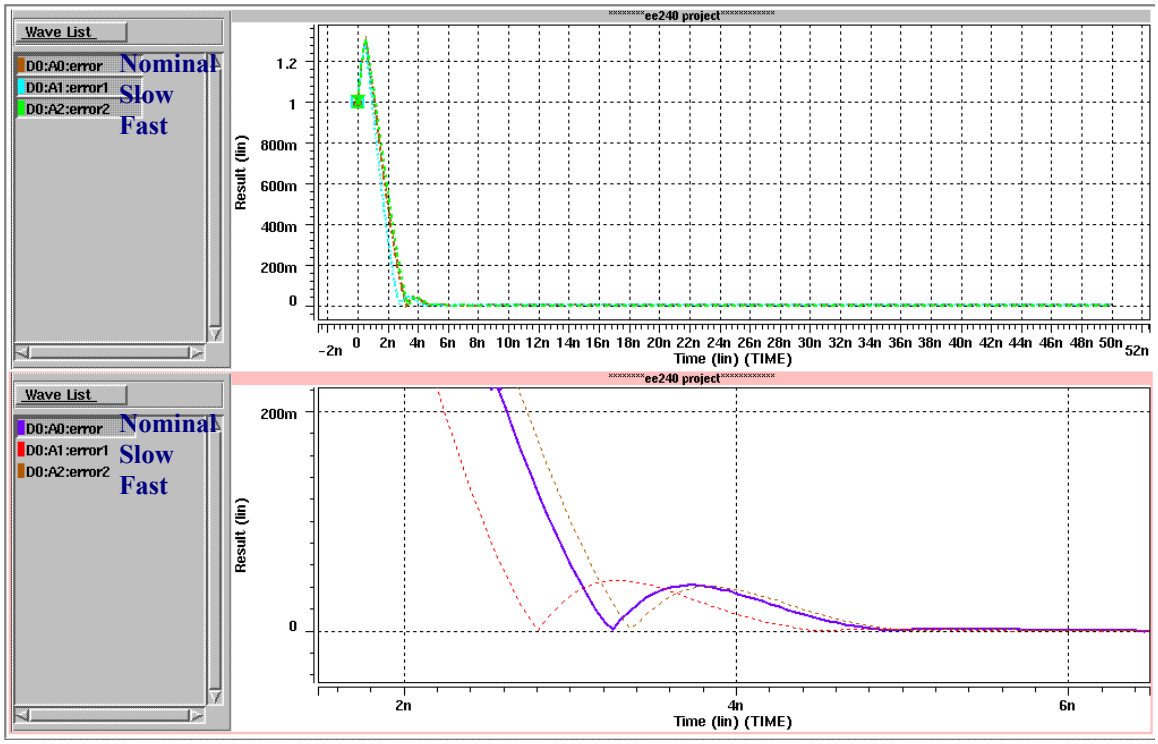


Figure 5.4.2 Settling Error ($V_{od} \rightarrow 1.8V$)

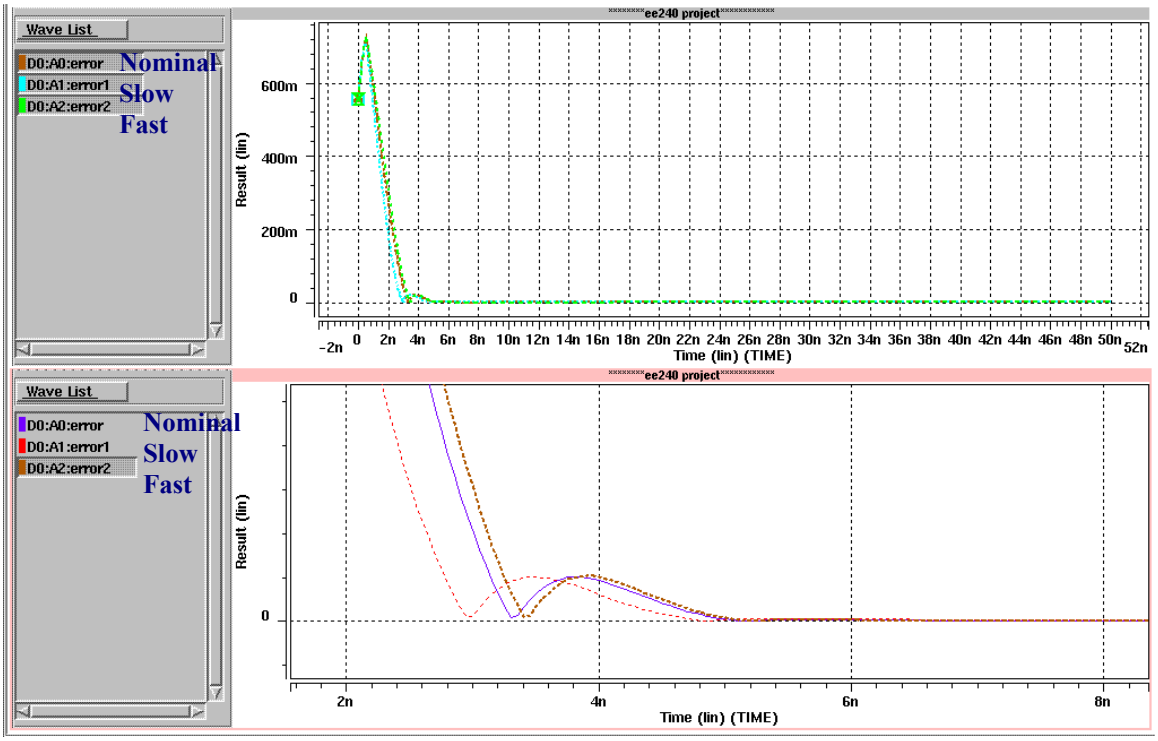


Figure 5.5.1 Power Dissipation in main amplifier and biasing (Vod=0V)

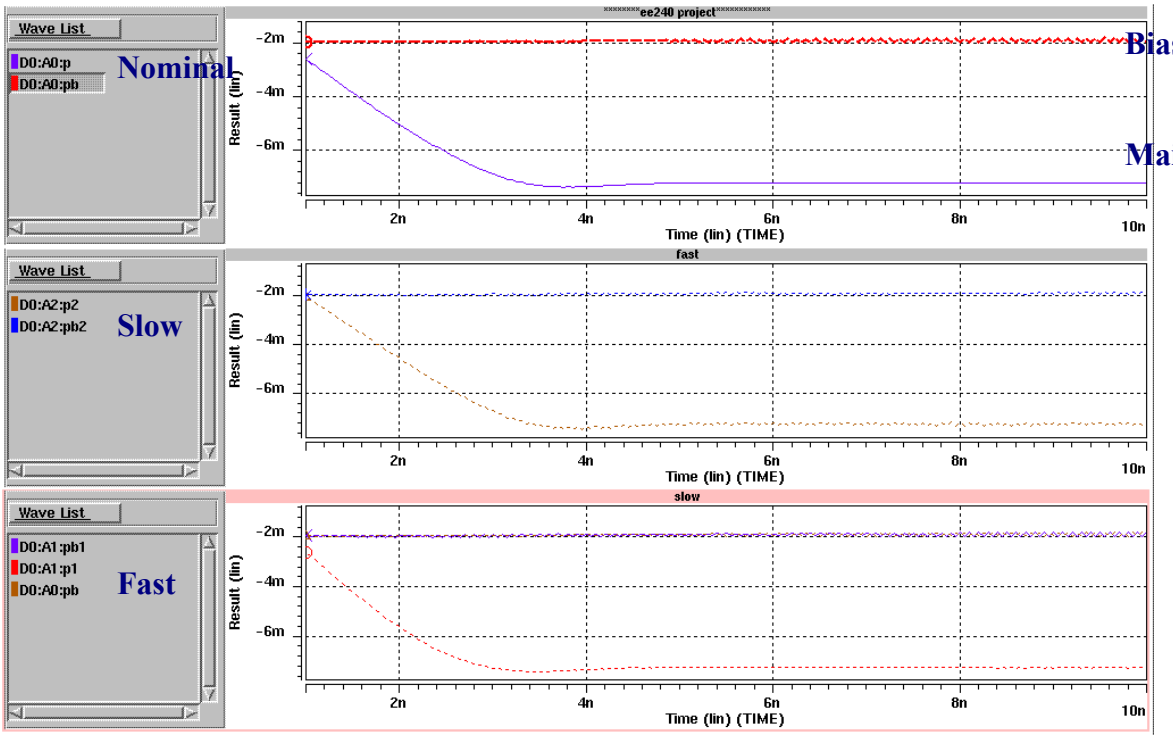


Figure 5.5.2 Power Dissipation in main amplifier & biasing (Vod=1.8V)

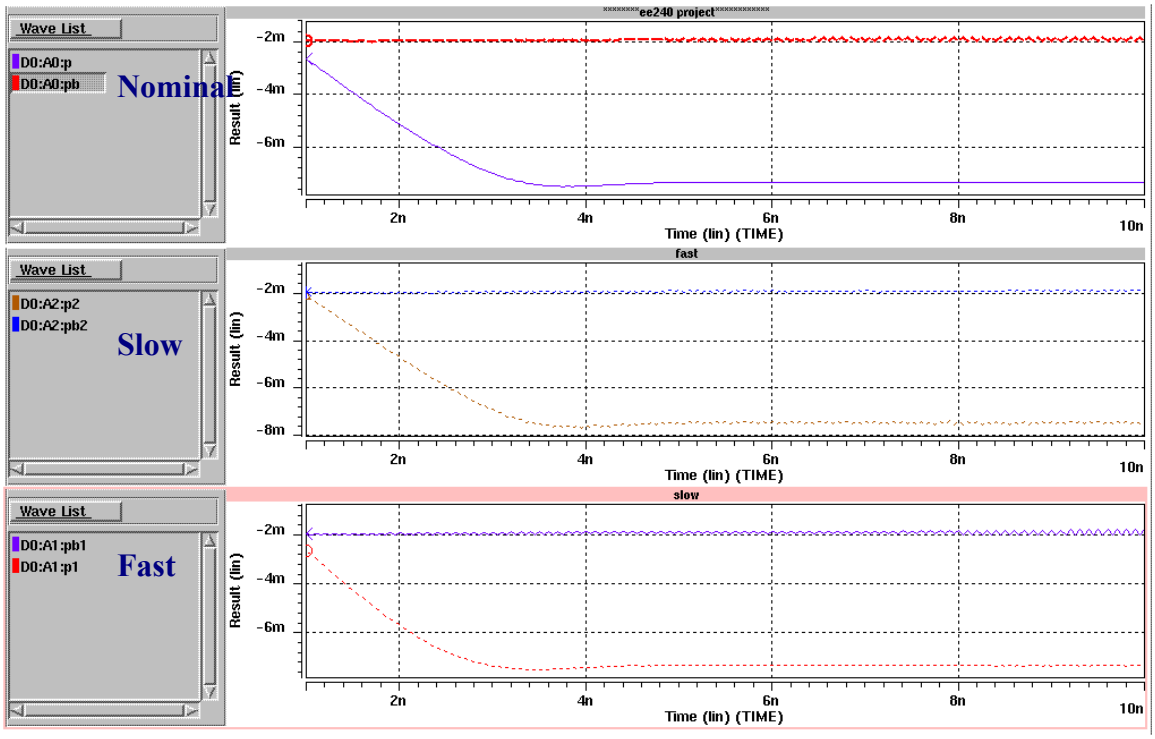


Figure 5.6.1 Noise Spectrum (Vod = 0V)

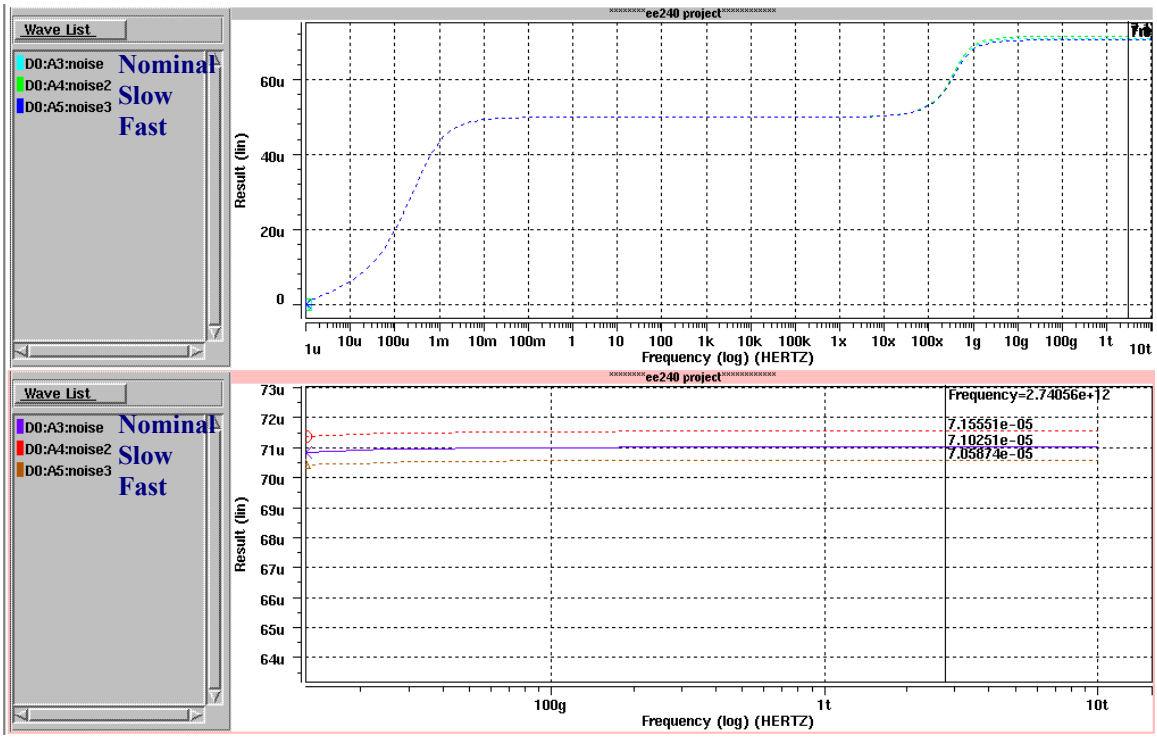
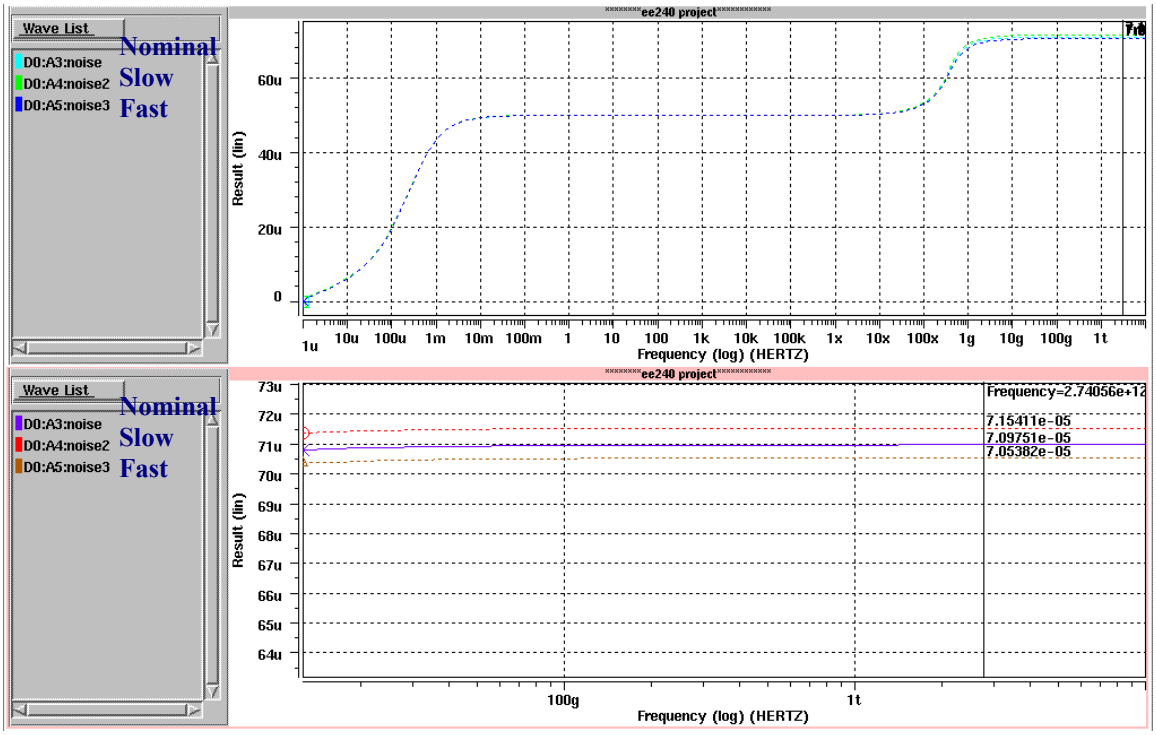


Figure 5.6.2 Noise Spectrum (Vod = 1.8V)



V. Comments and Conclusion

In our design and HSPICE simulation, we proven the design specifications have met. However we have assumed one-finger very large devices for each transistor. But in practice, there will be multiple fingers consideration for more area-efficiency. We have added well-to-substrate reversed-bias diode in the cascode to give us more realistic noise and transient simulations. Due to the fact that we do not use multi-fingers transistors for our simulation, the practical parasitics cannot be simulated. Some parasitic effects are not accounted for because they will contribute little effect on the results. For instance, the extra parasitic capacitors in bias circuits will slightly degrade the phase margin of the bias circuit but they act like bypass capacitance in the frequencies of interest. Some other parasitic capacitors are either tied to Vdd or Vss or ground and contribute no effect. However, the drain, source, gate and body parasitics are included and correctly simulated.

For the biasing network, we use 10:1 current ratio between transistors which is practical and any bigger ratio will cause significant mismatches. After all, all the specifications are met over all process corners while the main amplifier consumes 7.2mW of power and the bias circuits consumes1.9mW.

APPENDIX 1: DESIGN SPICE DECK

```
********EE240 Project************
VDD VDD 0 3V
VDD_B VDD_B 0 3V
IREF VDD_B BIAS1 120u

VID VID 0 DC 0 AC 1 PULSE (0 5 0 .5n .5n
50N 100N)
VIC VIC 0 DC .8V

XIN VID VIC Vi+ Vi- BALUN
XIN2 VD VIC Vx+ Vx- BALUN
XIN3 VD VIC Vy+ Vy- BALUN

.PARAM W1=500UM L1=.35UM
+      W3=800UM L3=1u
+      W7=800uM L7=1u
+      wbn=35u lbn=.35u
+      wbp=80u lbp=1u
+      w9=800uM l9=1u

**Tail current source***
mb1 vx cmfb_out 0 0  nmos w=w1 l=l1 m=2

***CFMB AMP***
mc1  dc1  cmfb  vxx  vxx   pmos  w=w7  l=l7
m=.33
mc2 cmfb_out vcmm vxx vxx pmos w=w7 l=l7
m=.33
mc3  cmfb_out  dc1  0  0   nmos  w=w1  l=l1
m=.033
mc4 dc1 dc1 0 0  nmos w=w1 l=l1 m=.033
rrr vdd_b vcmm 100t
rr2 vcmm 0 100t
crr vdd_b vcmm 500f
cr2 vcmm 0 500f
cc cmfb  0 4p

***Input transistors***
M1 d1 VX+ VX 0 NMOS W=W1 L=L1 m=1
M2 d2 VX- VX 0 NMOS W=W1 L=L1 m=1

***NMOS CASCODE
M3 Vo+ b1 d2 0 NMOS W=W3 L=L3 m=1
M4 Vo- b1 d1 0 NMOS W=W3 L=L3 m=1

***PMOS CURRENT SOURCE***
M7  D7 VB5 VDD VDD PMOS W=W7 L=L7 M=1
M8  D8 VB5 VDD VDD PMOS W=W7 L=L7 M=1
M9  VO+ VB6 D7 D7 PMOS W=W9 L=L9 M=1
M10 VO- VB6 D8 D8 PMOS W=W9 L=L9 M=1

***PMOS CASCODE WELL DIODES***
d9 0 d7 dwell a='(w9*13u)'
d10 0 d8  dwell a='(w9*13u)'

***HIGH SWING PMOS BIAS***
MB5 VB7 VB5 VDD_b VDD_b PMOS W=Wbp L=Lbp
M=1
MB6 VB5 VB6 VB7 VB7 PMOS W=Wbp L=Lbp M=1
MB7 VB8 VB6 VDD_b VDD_b PMOS W=Wbp L=Lbp
M=.25
MB8 VB6 VB6 VB8 VB8 PMOS W=Wbp L=Lbp M=1

***MAIN BIAS***
Mbias1  bias1  bias1  bias2  0  NMOS  W=Wbn
L=Lbn m=1
Mbias2 bias2 bias2 0  0 NMOS W=Wbn L=Lbn
m=1
Mbias3  bias3  bias1  bias4  0  NMOS  W=Wbn
L=Lbn m=1
Mbias4 bias4 bias2 0 0 NMOS W=Wbn L=Lbn
m=1
Mbias5 bias3 bias3 VDD_B VDD_B PMOS W=WbP
L=LbP m=1

***M3 AND M4 BIAS***
Mbias6  b1  bias3  VDD_b  VDD_b  PMOS  W=WbP
L=LbP m=1
Mbias7 b1 b1 0 0 nMOS W=3.75u L=1u m=1

***M7-9 BIAS***
Mbias8  vb6  bias1  bias5   0  NMOS  W=Wbn
L=Lbn m=1
Mbias9  bias5 bias2 0 0 NMOS W=Wbn L=Lbn
m=1
Mbias10  vb5  bias1  bias6  0  NMOS  W=Wbn
L=Lbn m=1
Mbias11 bias6 bias2 0 0 NMOS W=Wbn L=Lbn
m=1

***CMFB AMP BIAS***
Mbias12 vxx bias3 VDD_b VDD_B PMOS W=WbP
L=LbP m=.25

***FEEDBACK***
CF1 VO+ Vy-  4p
CF2 VO- Vy+  4p
CS1 Vy+ VI+ .8p
CS2 Vy- VI- .8p
RF1 VO+ Vy- 10t
RF2 VO- Vy+ 10t
RS1 Vy+ VI+ 50t
RS2 Vy- VI- 50t

***CMFB***
CCMFB1 VO+ cmfb 80f
CCMFB2 VO- cmfb 80f
RCMFB1 VO+ cmfb 10T
RCMFB2 VO- cmfb 10T

CL+ VO+ 0 3pF
CL- VO- 0 3PF
XOUT  VOD VOC VO+ VO- BALUN

.include ‘util.inc’

.noise v(vod) vid
*.dc vid -3m 3m .01m
.TRAN .01N 10N
.ac dec 10 1u 10t
*.probe vdb(tv) p(tv) vdb(ti)
*.tf v(vod) vid
.model  dwell  d  cj0=1e-4  is=1e-5  m=0.5
bv=40
.op
.options dccap post=2  brief
.lib 'cmos35.txt' nominal


.alter slow
.lib 'cmos35.txt' slow
.alter fast
.lib 'cmos35.txt' fast
.end
```