Low Power Gbit/sec Low Voltage Differential Signaling I/O System

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Abstract

The effects that I/O circuits have on the overall system performance are becoming more and more pronounced nowadays, as many digital processors reached GHz frequency range while I/O operates only up to MHz range. Extensive studies have been done on I/O signal processing and multi-clocking schemes to increase number of bits per Hz of transmission. In this paper, a circuit level approach to this problem is presented, in particular a low voltage differential signaling (LVDS) interface circuitry is investigated. Simulations have shown 3.0Gbit/sec transmission rate is achieved in a 0.18µm technology while transmitter and receiver dissipate less than 20mW and 25mW power respectively.

Introduction

In today’s digital system, clock frequency of digital processor has reached multi-GHz range and up, while frequency of I/O circuits only operates up to MHz range due to circuits and transmission line limitations. As a result, overall global performance is significantly limited by I/O circuits rather than circuits at the core level and silicon process technology. [1] As CMOS technology continues to take enormous progress, this issue will be more noticeable in the near future. Therefore we call attention to the study of I/O interface with a low voltage differential signaling (LVDS) I/O circuitry which allows clock frequency operate up to GHz range, despite lossy transmission line and unintentional improper transmission line termination.

In the Analysis and Results section, high performance LVDS I/O system is first considered, then followed by LVDS power analysis and finally additional operations of LVDS system are introduced.

I/O Architectures

The most straightforward conventional I/O driver is a chain of inverters driver and receiver configuration (Figure 1) which is simple, has wide noise margins, and does not dissipate static power.

![Figure 1. Conventional I/O Inverters Chain](image-url)

However this approach cannot achieve the highest performance and lowest possible power because interconnection must be driven between $V_{dd}$ (power) and $V_{ss}$ (ground). Besides, the receiving inverter does not respond until its input reaches the switching point which is approximately $V_{dd}/2$. In addition, ESD (Electro Static Discharge) protection
presents parasitic, making the signal delay suffer more severely.

In addition, single-ended signaling would also result in uncontrolled high-speed return currents flowing in supply and/or ground plane in the system. Therefore, the conventional approach is quite unsuitable for high-speed low-power applications.

**Differential Methods**

The large voltage swing on the signal line is one of the speed and power limitation factors. For power enchantment, a lower voltage swing level can be considered, but the noise margin gets deteriorated immediately.

To compensate the possible performance degradation, differential signaling methods have been exploited. Differential signals are immune to common-mode noise and any issues of shifting DC levels are furthermore cancelled out when differential signals are used. However, differential signal amplitudes must be high enough to secure noise margin since signal amplitude decreases with transmission distance.

**LVDS Link**

A typical LVDS link is shown in Figure 2. It consists of three main components as in many other I/O systems: (a) a source/transmitter to drive the signal differentially to propagate across the interconnects, (b) two transmission lines for the differential signal propagation, and c) a differential receiver that senses the difference in the signals between the two transmission lines and converts the differential signal into full rail-to-rail digital output data.

![Figure 2. Typical LVDS link. [6]](image)

**LVDS Operations**

**Transmitter**

The simplified version of the fully differential LVDS transmitter is illustrated as switches in Figure 3. The transmitter essentially acts as a current steering switch that can source and sink current simultaneously to and from the pair of interconnects. Four MOS switches are constructed in a bridge configuration and each cross-opposite pair is connected to the full rail-to-rail digital input signal and its complementary signal respectively.

![Figure 3. Simplified switching model of the LVDS fully differential transmitter [17]](image)
**Receiver**

The receiver is implemented as a high gain differential pair amplifier, followed by buffers. The 100-Ω resistor shunting the two transmission lines at the input of the receiver acts as both the termination and load resistance, converting current sourced by transmitter into a small differential voltage. The receiver then senses this small differential signal voltage and amplified it into a rail-to-rail digital signal to the core circuit.

**Transmitter Line Model**

Transmission line model used in simulations is the RGLC model as featured in fig. 4. In our simulation setup, wire length of 1cm, propagation speed of 15cm/ns (SiO₂), capacitance per unit length 200pF/m and inductance per unit length 500nH/m are used. This setup gives characteristic line impedance of about 50Ω.

![Figure 4. Transmission line model [13]](image)

However resistance plays an important role [13] in I/O performance, thus a lossy transmission line is used to simulate I²R and skin effect (−3dB at 1GHz) losses.

At this point we should emphasize the fact that even though simulations are done for on chip silicon inter-module communication, all results apply to PCB and long distance AWG twisted pair communication since a “pessimistic” loss in link is accounted for a 1cm wire.

**Other Simulation Considerations**

There are many other simulation considerations taken with the most noticeable one is the fact that we have simulated well-grounded substrates on both receiver and transmitter ends. In a typical communication system different ground levels at both end could lead to inferior overall performance. Due to the differential nature of LVDS, common mode noise rejection is extremely high so noise coupling in transmission is not accounted for. Input voltage offset in receiver is not taken into consideration; however trimming can be done easily to minimize this non-ideality.

To appreciate the speed improvement, SPICE simulation is performed on both I/O circuits (figs.1 and 2) driving a properly terminated transmission line, with characteristics impedance, $Z_o$ of 50Ω. Improved variations of the SA receiver are designed, compared and studied as well.

The LVDS voltage levels used in all simulations are specified by IEEE [12]

**Analysis and Results**

**High Speed Design**

The key to high performance LVDS design is to realize a fast switching network of the driver and a high gain, fast respond receiver sense amplifier.

To achieve the first criteria, transistors must be sized carefully to handle the reference current $I_{ref}$ fig. 5 which flows through the transmission line. In addition to that, driver transistors must handle the reflection waves and current $I_{reflection}$ if not line is not properly terminated.
Parasitics effect and area set the upper size limit of transistors while lower limit is set by the line capacitance driven, breakdown issue and the on resistance $R_{ds(on)}$ of transistors. Common mode voltage must also be defined through the use of feedback such that receiver transistors are biased correctly.

![Figure 5. Transmitter Schematics (common feedback circuit not shown in figure)](image)

At the receiver end, to ensure fast signal propagation, a high gain sense amplifier is considered. Sense amplifier utilizes differential pair input network, biased with $I_{tail}$. It can be shown that when

$$V_{id} = \sqrt{2(V_{GS} - V_t)}$$  \hspace{1cm} (1)

all of the tail current, $I_{tail}$, flows to one side of the differential pair, allowing maximum current for slewing and thus minimum delay for given power dissipation.

With this in mind, for an ideal long channel device

$$V_{d_{sat}} = (V_{GS} - V_t)$$  \hspace{1cm} (2)

is chosen for a given differential voltage at the receiver end $V_{id}$ which equals to $I_{ref} \times R_T$. From equations (1) and (2), and based on ideal square law behave, $V_{d_{sat}}$ of 140mV should be used $V_{id}$ of 200mV.

However to account for velocity-saturated devices which suffer from transconductance gain degradation, a smaller overdrive $V_{d_{sat}}$ should be chosen in order to minimize linear region, allowing fast conversion from small differential input voltage to rail-to-rail digital logic. With this in mind, a 100mV overdrive voltage is chosen for the receiver in our design and any further decrease will lead transistors to operate in weak inversion which gives inferior and less optimal performance. Logical effort/fanout-of-4 inverter sizing technique is used at the output of differential sense receiver to further restore level signal.

![Figure 6. Simulations of LVDS I/O system, output rail-to-rail signal (top) and input differential signal (bottom)](image)

Simulation shows differential line voltage of 200mV and receiver output gives rail-to-rail digital signal while frequency of GHz range is easily achievable.

Additional results are generated in SPICE simulation where the termination
resistance is varied. The plot in fig. 7 shows the result of the delays as termination resistance value derivates from the line characteristic impedance. As supposed to I/O buffer chains of fig. 1, LVDS system shows very little variations as $R_T$ varies unintentionally possibly by means of ESD damage or devices mismatches. Results clearly indicate the robustness of LVDS in this aspect.

**Power Saving**

To get a sense of how much power saving can be realized in LVDS interface, dynamic and static power consumption of LVDS and conventional buffer chain I/Os are compared in fig. 8. Although LVDS consumes static power due to class-A amplifiers in transmitter and receiver, a huge dynamic power saving is readily realized when the LVDS driver only needs to drive low-swing signals across the links (order of 100’s mV).

Furthermore, the dynamic power consumption scales with the supply voltage ($\propto V_{DD}^2$) for conventional single ended I/O buffer chains because the signal is driven rail-to-rail. (fig. 9) Dynamic power in differential signaling scheme in LVDS is independent of supply voltage as long as it can steer a constant current in and out of the impedance load.

**Additional LVDS Interface**

**Single-Ended LVDS**

In a less noisy environment, LVDS interface can also be implemented as a single-end I/O system driving one
transmission link. However special care must be taken in a sensitive system like this. Common mode voltage must be carefully and precisely defined in both driver and receiver. Any mismatches will cause erroneous data transmission. Even though simulation results are very much operational (fig 10), noise coupling issues must be controlled very carefully (not simulated) when applying single-ended LVDS transmission.

Figure 10. LVDS driving a single transmission line – the top graph shows a small signal sitting on a dc reference voltage, and the bottom graph shows buffered rail-to-rail digital signal retrieved at the output.

Level Shifting

LVDS interface permits different power supply levels between the transmitting side and the receiving end. While serving as an interface between different voltage domains, LVDS I/O circuit must not lose much of the speed and power performance. Both transmitter and receiver can be tied to different supply rails as long as they can reliably drive and sense the small differential signal respectively. Simulations have shown there is virtually no speed penalty while static biasing current is easily scaleable down when higher Vdd supply is used.

Figure 11. Inherent level-shifting property of the LVDS interface is shown in simulations.

Conclusion

The operation of a low power and high speed digital LVDS I/O circuitry is demonstrated to be operational up to 3Gbit/sec. This high performance and low power I/O interface is very appealing to most short and long distance inter and intra-chip communications. Like any other I/O system, a LVDS interface circuit must demonstrate robustness, and immunity to noise and ESD. However unlike most systems, LVDS has a lot more flexibility, namely in the voltage margin domain. With 1.8V Vdd and 200mV differential voltage swing, only about 11% of voltage headroom is utilized, giving rise to more judicious voltage margin budgeting scheme. The high speed and low power technique featured in this paper can be easily applied to multi-voltage level, multi-clock, multi-channel and bi-directional I/O systems while only a pair of transmission line is required.
References:


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