MIT 3.155/6.152

MOSCAP mask layout, testing and analysis procedure

September 2006

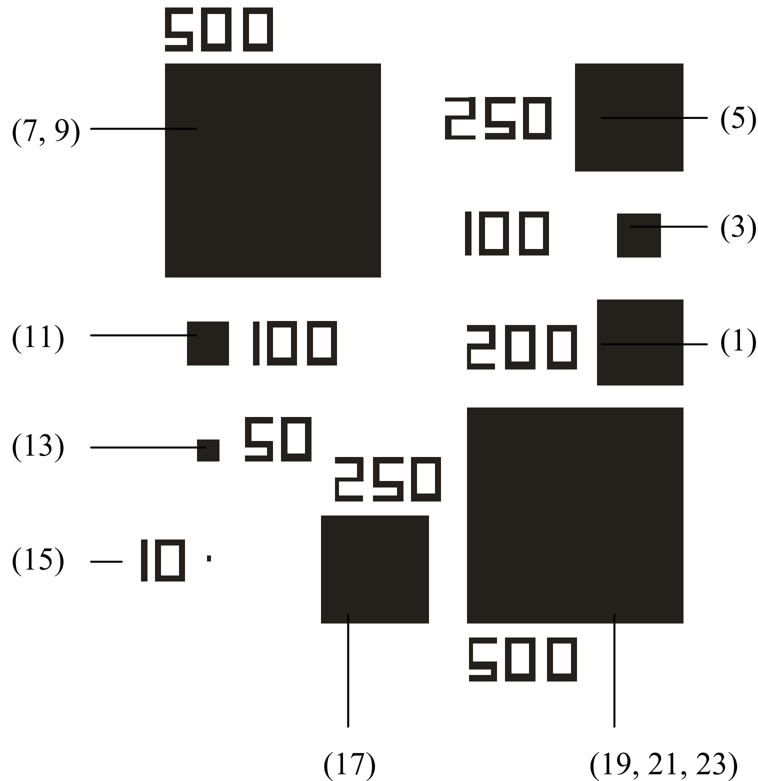
There are three types of test site on the MOSCAP mask:

1. one containing a variety of square capacitors with side lengths ranging from 10 to 500 µm;
2. one with a large van der Pauw test device, for determining polysilicon sheet resistance;
3. one with a smaller van der Pauw test device, plus 32- and 64-square polysilicon resistors.

Each site is designed to have electrical contacts made to it using a probe card with 12 pins in a fixed physical arrangement (they are not numbered consecutively). The wafer is positioned on the probe station and all probes are lowered on to the test site simultaneously. Electrical test apparatus is connected to the probes using interchangeable leads.

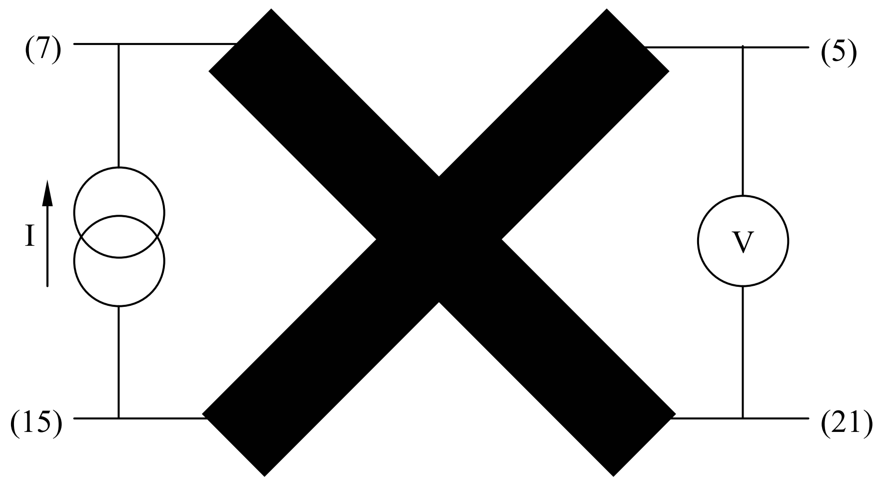
Site 1

Shaded squares represent polysilicon remaining on the device surface. The side-length of each capacitor is given in microns. Probe pin numbers are annotated in parentheses.



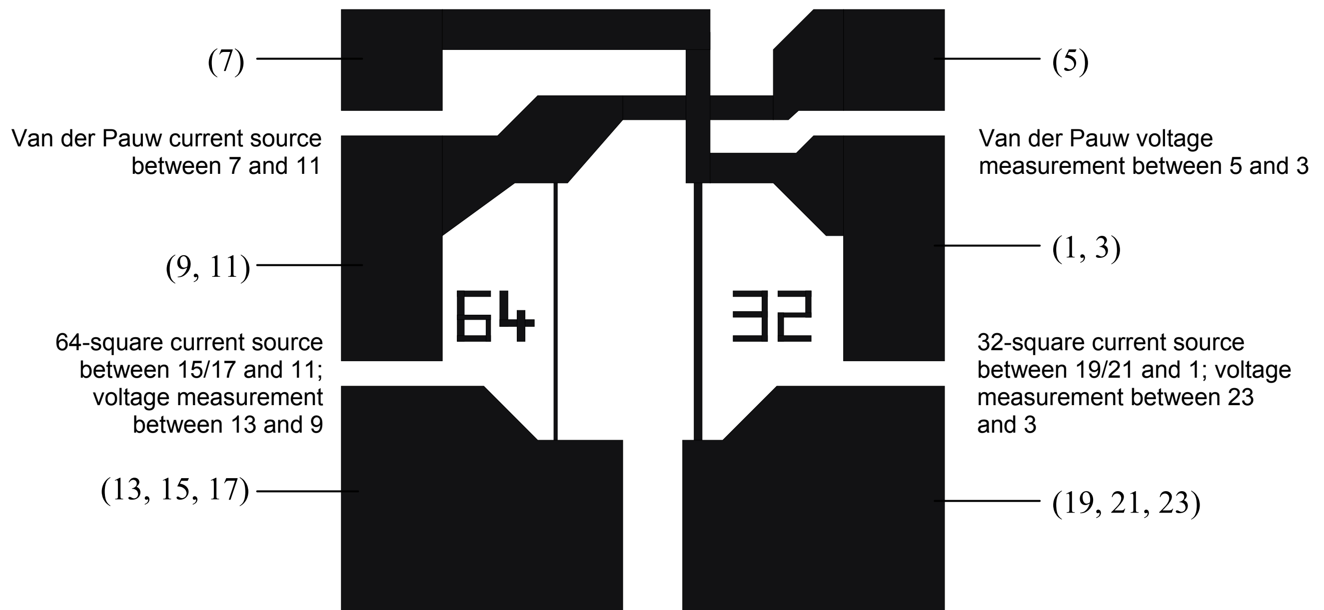
Site 2

Van der Pauw test site for polysilicon sheet resistance



Site 3

Van der Pauw test, plus 32- and 64-square resistors

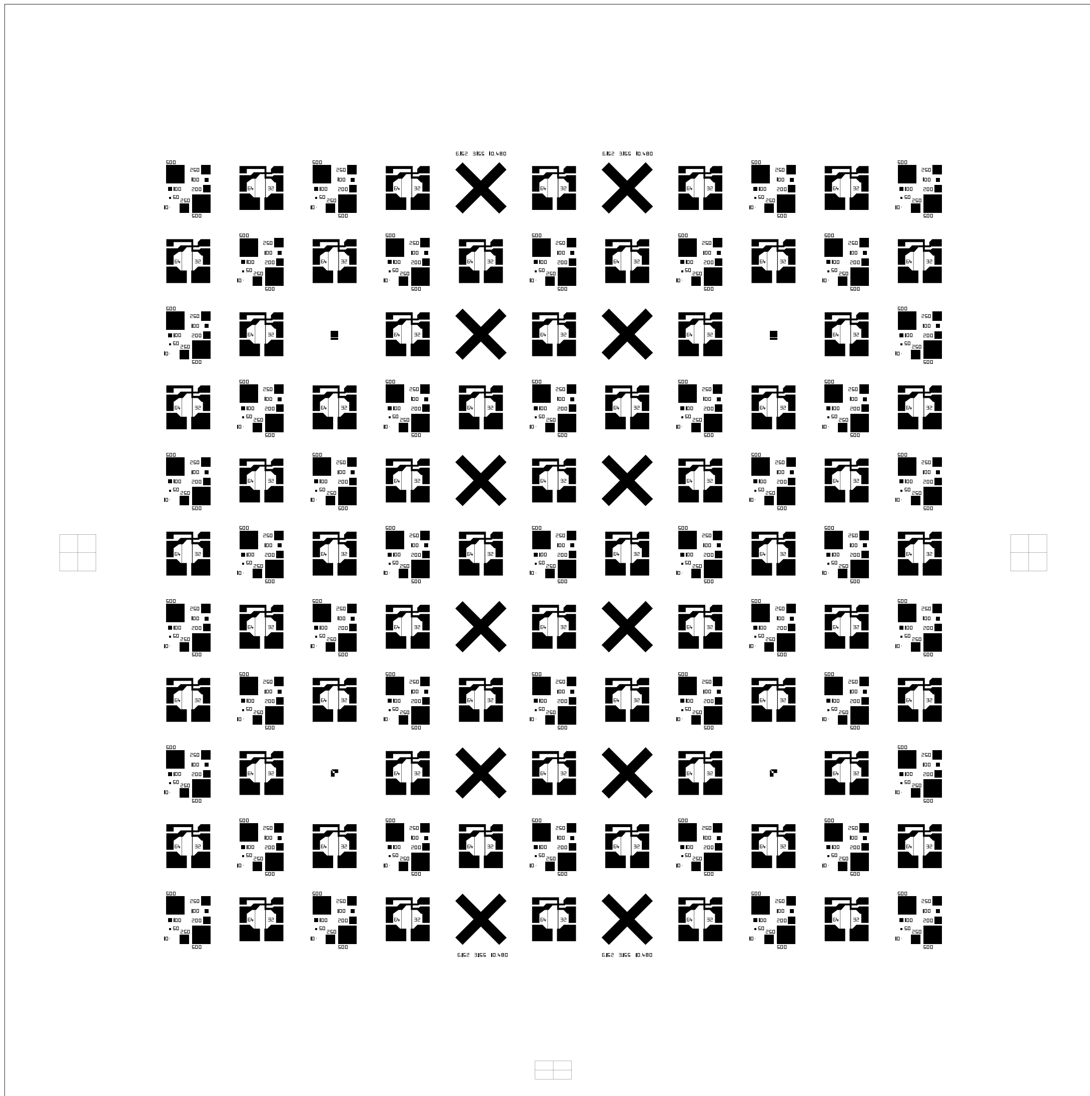


32-square resistor: nominal width, 16 µm
64-square resistor: nominal width, 8 µm

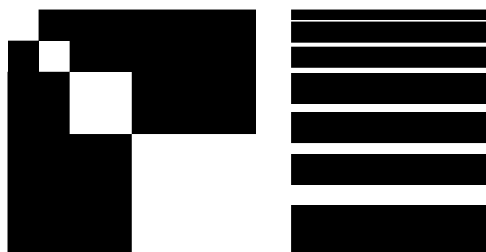
Pins 13, 15 and 17 can also be used to determine the contact resistance of the probes.

Overall reticle

The whole die is 20 mm on each side when it appears on the wafer, and the die is repeated in a grid across the wafer; each site within the die is about 1.5 mm on each side. The design of the reticle placed in the i-Stepper is shown below (features on the reticle are 5 times the size they will appear on the wafer). Reticle alignment marks are shown near the edges of the reticle.



The die also contains squares with abutting corners and lines with spaces down to 2 microns — for assessing the quality of exposure of photoresist:



Testing

The tests that will be undertaken are listed in the table below. The procedure for the C–V tests is to make contact with the polysilicon capacitor plate of interest using pin 1. The back-side of the wafer, meanwhile, is grounded. A 1 MHz ac signal is then superimposed on a dc bias that is swept at ~ 1 V/s between –5 V and 5V, applied across the capacitor. As the bias changes, the small-signal capacitance is repeatedly determined by the apparatus. With this particular set-up, the bias usually begins at –5 V and increases in steps of 50 mV, although there are two exceptions: tests 4 and 5.

All resistance measurements involve passing a varying, controlled current through the test device using one pair of probes (SMU1 and SMU2), and measuring the induced voltage across the resistor with a second pair of probes (VM1 and VM2). The magnitudes of the currents and the positions of the probes are given in the table.

The test rig is also equipped with a lamp and a tube positioned over the probe locations that can deliver a stream of nitrogen to the surface of the wafer.

Test #	Type	Structure	Nitrogen flow	Light	Notes
1	C–V	(500 μm)^2 capacitor	off	off	Control
2			on	off	Test effect of nitrogen
3			off	on	Test effect of illumination
4			on	off	Reverse direction of bias voltage sweep: go from 5 to –5 V in ~20 s.
5			on	off	Reduce voltage step to 5 mV
6		(200 μm)^2 capacitor	off	off	
7			on	off	
8		(100 μm)^2 capacitor	off	off	
9			on	off	
10		(50 μm)^2 capacitor	off	off	
11			on	off	
12		(500 μm)^2 cap.	on	off	Wafer whose polysilicon has been additionally sintered at ~400 °C for several hours *after* plasma processing.
13		(200 μm)^2 cap.	on	off	
14	van der Pauw sheet resistance (use a current source of –10 mA)	Site 2	off	off	SMU1: 7 SMU2: 15 VM1: 21 VM2: 5
15	32-square resistance	Site 3	off	off	Intended connections: SMU1: 7 SMU2: 15 VM1: 21 VM2: 5 Improved? (with pins moved*): SMU1: 21 SMU2: 5 VM1: 23 VM2: 3
16	64-square resistance	Site 3	off	off	Intended connections: SMU1: 7

					SMU2: 15 VM1: 21 VM2: 5 Improved? (with pins moved*): SMU1: 21 SMU2: 5 VM1: 23 VM2: 3
17	Contact resistance	Site 3	off	off	SMU1: 13 SMU2: 15 VM1: 17 VM2: 15

* To bring the voltage measurement locations closer to the ends of the resistors, this arrangement, which involves moving the pins across the test site, is proposed.

Data

C–V curves and extracted resistances from each lab session will be posted on the course website.

Site 3 analysis

Site 3 includes two polysilicon resistors — 32 and 64 squares in shape — plus a van der Pauw test pattern: a cross.

Sheet resistance measurements

The sheet resistance of the polysilicon can be estimated, independently of any small, unintentional variations of critical dimensions, by using the van der Pauw pattern:

$$R_{\square} = (\pi/\ln 2)(V/I)$$

where $R_{\square}$ is the resistance per square, V is the voltage measured across two adjacent branches of the pattern, and I is the current passed between the other two adjacent branches. Initial tests suggest a sheet resistance of 138.9 Ω/sq, or 3.47×10^{-3} Ω-cm.

Critical dimension deviations

If we wish to estimate the impact of any photolithographic and etching imperfections upon the dimensions of the final polysilicon patterns, we can use the resistors.

One way to estimate variations of critical dimensions is to measure the value of one of the resistors, and divide that by the sheet resistance (obtained using the van der Pauw test), to give the magnitude of the resistance in terms of ‘squares’. If the measured number of squares is greater than nominal number

of squares, we could interpret that as showing that the processing has caused polysilicon features to shrink — perhaps because of overexposure of the photoresist, or unwanted etching of the polysilicon under the edges of the photoresist.

Another possible way of estimating critical dimensions' variations is to compare the values of two resistors with different shapes. On test site 3, we performed 4-point resistance measurements on both resistors, which are nominally 64 and 32 squares in shape and yield measured values R_1 and R_2 respectively. If the widths of both resistors are increased from the dimensions on the mask by a constant ΔW (and the lengths are concomitantly reduced), we can write

$$R_1 = \frac{\rho}{t}\left(\frac{L - \Delta W}{W_1 + \Delta W}\right)$$

and

$$R_2 = \frac{\rho}{t}\left(\frac{L - \Delta W}{W_2 + \Delta W}\right)$$

where ρ is polysilicon's resistivity, t is its thickness, L is the nominal length of both resistors (before variation of dimensions) and W_1 and W_2 are the nominal (mask) resistor widths ($W_2 = 2W_1$).

Let $\beta = R_2/R_1$;

then $\Delta W = (\beta W_2 - W_1)/(1 - \beta)$.

We could thus make an estimate of ΔW independently of our estimate of sheet resistance, and compare it to that obtained using just one of the resistors in conjunction with the van der Pauw test.

Initial data from the 4-point tests suggests the nominally 64-square resistor has a resistance of 9.75 kΩ, or 70.2 squares, while the nominally 32-square resistor has a resistance of 5.34 kΩ, or 38.4 squares.

Using the first method, the 64-square resistor would indicates a ΔW of 1.4 μm, while that of the 32-square resistor would indicate a ΔW of 2.7 μm. But using the method involving both resistors implies a β of 1.828 and a ΔW of

(1.828 * 32 μm – 16 μm)/(1–1.827) = –51.3 μm

which is impossible, since the nominal widths of the resistors are only 16 and 32 μm.

It seems likely that the source of the discrepancy is that the voltage probes were not close enough to the 32- or 64-square gauge lengths during testing, to that the resistance measurements include a component from the resistance of the pads. β (which ought to be >2 for a positive ΔW) is therefore

Optical measurements

The patterned polysilicon has been measured optically, and resistor widths were found to vary by no more than 1 μm from the nominal widths of 8 μm and 16 μm, for the 64- and 32-square resistors respectively. The step height of features on the wafer has been measured using optical interferometry to be 300 ± 20 nm, whereas the target poly deposition thickness was 250 nm and the thickness measured using an ellipsometer in the ICL was ~ 230 nm. It is possible that some of the oxide was etched during processing, increasing the step height to be greater than the poly thickness, but the gate oxide thickness is only ~50 nm so this would mean that the whole oxide layer had been etched through.