# Fast simulation of pattern dependencies in thermal nanoimprint lithography

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# Nanoimprint modeling needs

#### Experiment



0.1 mm

RLT

(nm)

200

80

## • Cell-level

- Hundreds of features
- Guide iterative layout design
- Desktop processing in minutes

### Chip-level

- Many millions of features
- Pre-fabrication check: overnight?
- Guide process selection

## Need for flexibility

- Rapid innovation in resist and stamp materials
- Richness of geometries

# We need a unified simulation approach for micro- and nano-embossing/imprinting



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Initial polymer thickness,  $r_0$ 

## Key: model impulse response g(x,y,t) of resist layer



After Nogi et al., Trans ASME: J Tribology, 119 493-500 (1997)

### Change in topography is given by convolution of impulse response with pressure distribution





## **Contact pressure distributions can be found** for arbitrary stamp geometries

2.3 µm-thick polysulfone film embossed at 205 °C under 30 MPa for 2 mins

Stamp design . . . . Cavity 160 MPa Ω

#### Simulated pressure

#### **Optical micrograph**



200 µm

Taylor et al., SPIE 7269 (2009).

# Successful modeling of polysulfone imprint

2.3 µm-thick polysulfone film embossed at 205 °C under 30 MPa for 2 mins



Taylor et al., SPIE 7269 (2009).

## **Representing layer-thickness reductions**



• Material compliance J(t)

$$p_{g}(x, y, t_{h}) = (1 - \nu^{2}) \int_{0}^{t_{h}} p(x, y, t') \frac{\mathrm{d}J(t - t')}{\mathrm{d}t'} \mathrm{d}t'$$

# Modeling stamp and substrate deflections



#### **Elastic point-load responses**



# **Modeling stamp and substrate deflections**



## **Simulation method: step-up resist compliance**

### PMMA 495K, c. 165 °C, 40 MPa, 1 min Experiment



## Abstracting a complex pattern

Local relationships between pressure-compliance and RLT:



# Simulation results: abstracted pattern

3 min 5 min



Simulated residual layer thickness



495K PMMA, 10–15 MPa, 170 °C



## **Simulation time**







Stamp 1 Feature-scale



Stamp 2 Abstracted

## **Strengths of the simulation method**

#### A unified simulation approach

- Can cope with any layer thickness
- Can integrate feature sizes ranging over many orders of magnitude
- Can model any linear viscoelastic material
- Speed
  - At least 1000 times faster than feature-level FEM
- Implicit periodic boundary conditions are useful
  - Realistic representation of whole-wafer imprint of many chips
  - Can use edge-padding for non-periodic modeling

### Suited to quick adaptation for new NIL configurations

- Use to explore the use of flexible stamps and substrates
- Explore the imprinting of non-flat substrates
- Micro-contact printing; roll-to-roll

## Varying stamp's bending stiffness: simulations



# Summary: fast nanoimprint modeling

#### Experiment



Simulation

0.1 mm

**RLT** 

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## Contributions

- Flexible modeling approach
- Pattern abstraction optional
- Suited to cell and chip scales
- 1000+ times faster than FEM

#### Outlook

- We will need NIL-aware design checking
- Can use as an engine for "Mechanical Proximity Correction"

# Acknowledgements

#### Funding

• The Singapore-MIT Alliance

#### Colleagues

 Matt Dirckx, Eehern Wong, Melinda Hale, Aaron Mazzeo, Shawn Chester, Ciprian Iliescu, Bangtao Chen, Ming Ni, and James Freedman of the MIT Technology Licensing Office

#### Helpful discussions

 Derek Bassett, Roger Bonnecaze, Siddharth Chauhan, Grant Willson, Yoshihiko Hirai, Wei Wu, Roger Walton, and John Mutkoski