Modeling and mitigating pattern and process dependencies in nanoimprint lithography

23 June 2011

Hayden Taylor
Singapore-MIT Alliance for Research and Technology

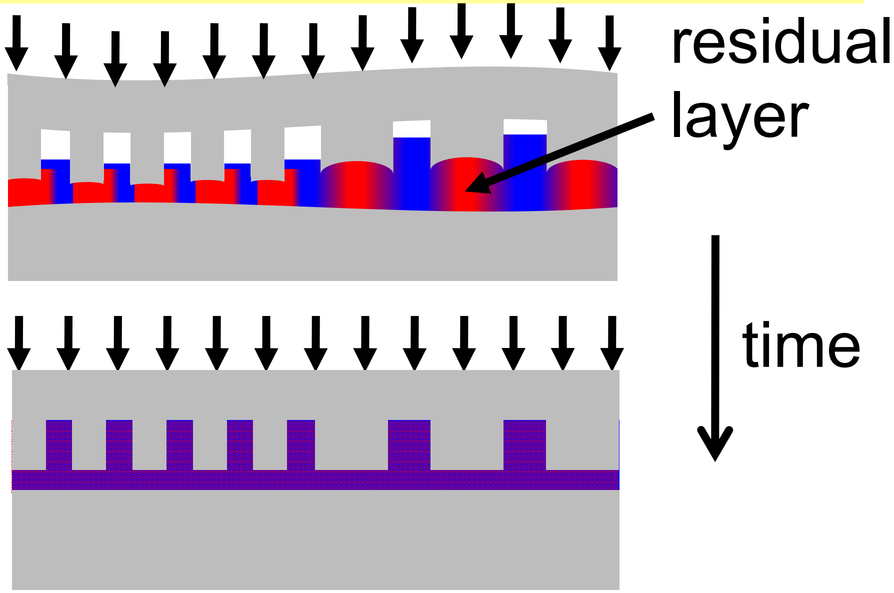
formerly based at:
Microsystems Technology Laboratories, MIT

Collaborators and acknowledgements

- **Funding**
  - Singapore-MIT Alliance
  - Danish National Advanced Technology Foundation
- **NIL Technology**
  - Kristian Smistrup
  - Theodor Nielsen
  - Brian Bilenberg
- **University of California, San Diego**
  - Andrew Kahng
  - Yen-Kuan Wu
- **MIT**
  - Duane Boning
  - Cai Gogwilt
  - Matt Dirckx
  - Eehern Wong
  - Melinda Hale
- **Helpful discussions**
  - Hella Scheer
  - Yoshihiko Hirai
  - Dave White

Spun-on *vs* droplet-dispensed resist in NIL

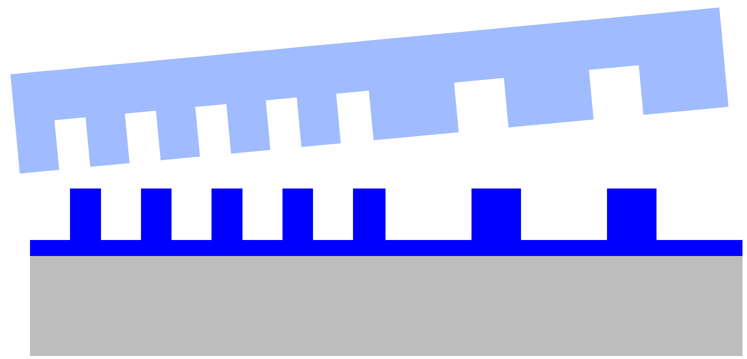
Spun-on resist



– Resist viscosity ≥ 10^3 Pa.s
– Applied pressures ~ 5 MPa
– Thermoplastic or UV-curing
– Viscous resist squeezing
– Elastic stamp deflections

S.Y. Chou *et al., Appl. Phys. Lett.* vol. 67 pp. 3114-3116, 1995
S. Fujimori, Jpn. J. Appl. Phys. vol. 48 p. 06FH01, 2009

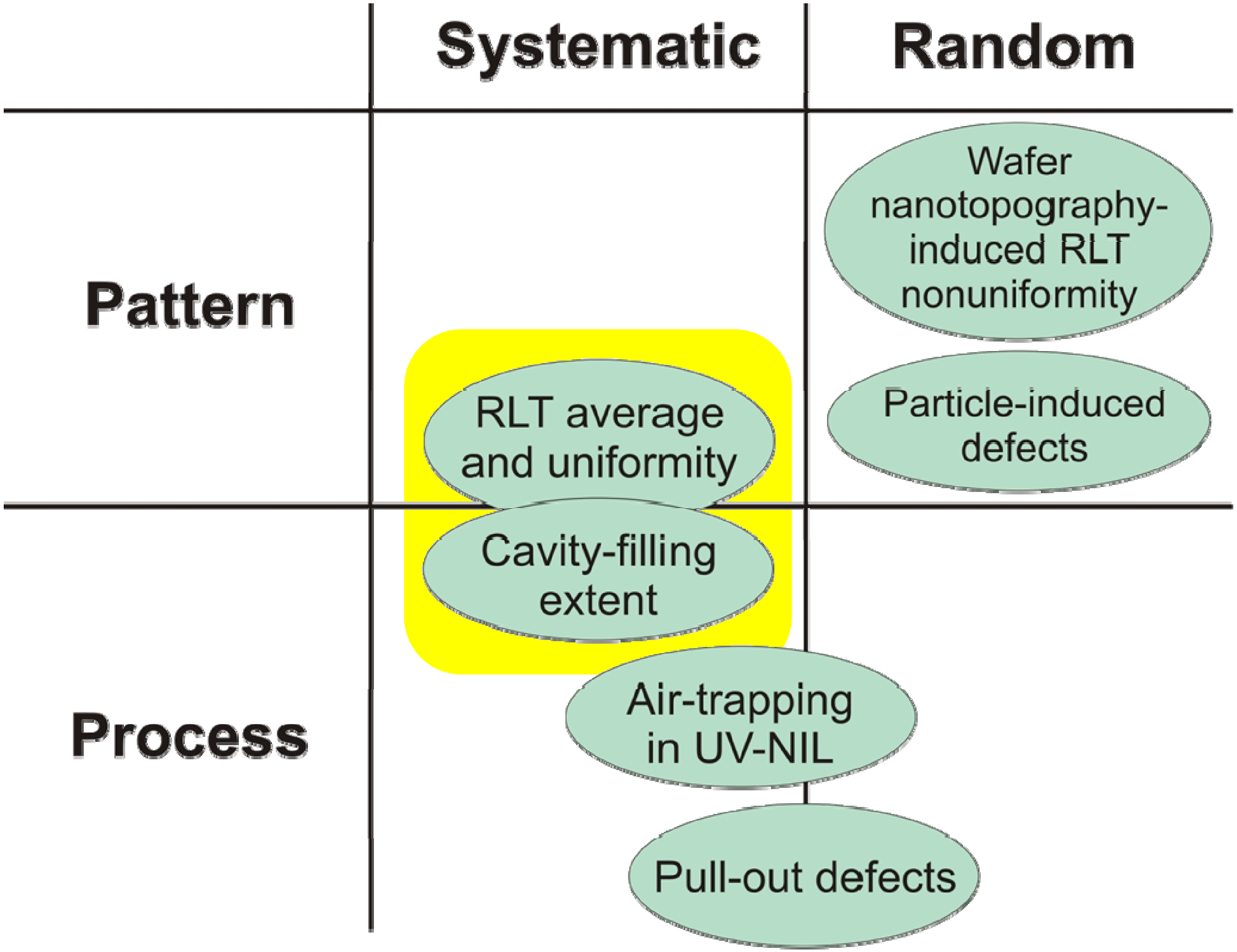
Droplet-dispensed resist



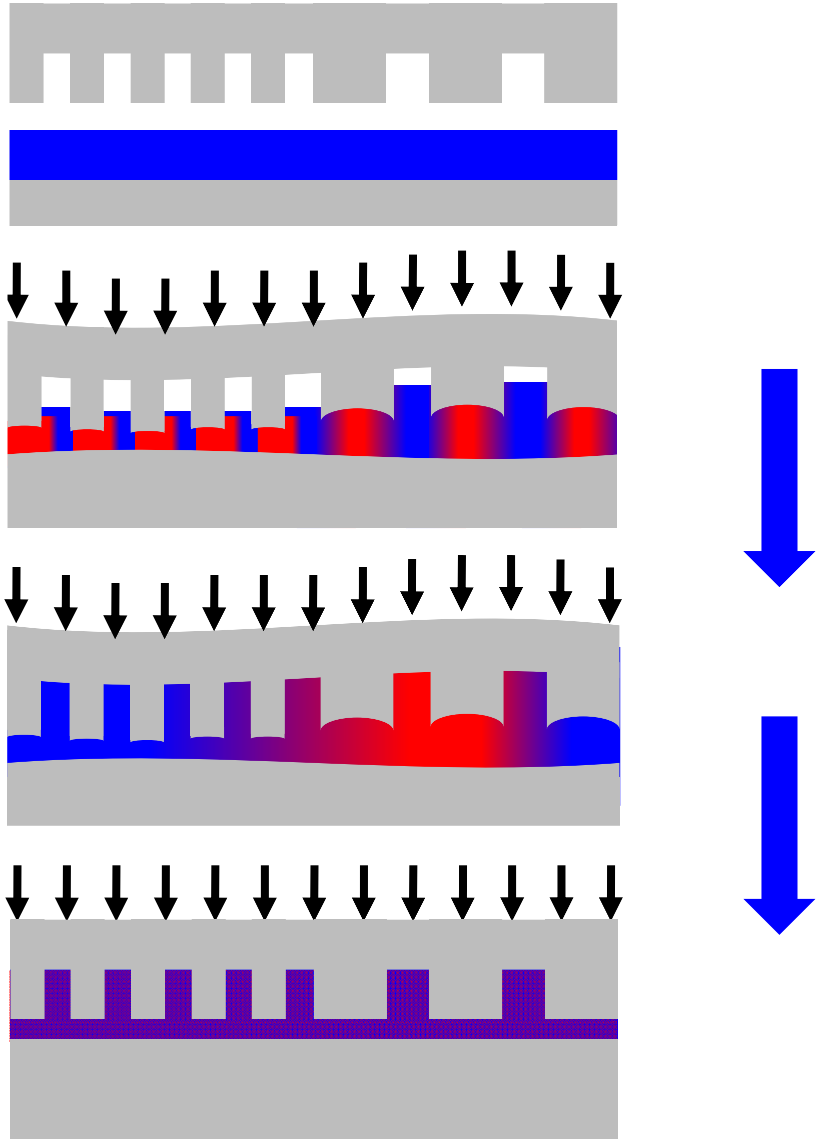
– Resist viscosity < 0.1 Pa.s
– Applied pressures ~ 5 kPa
– Droplets tailored to pattern
– Key figure of merit: filling time
– Gas trapping and dissolution

M. Colburn *et al.*, SPIE 3676, pt.1-2, 379-89, 1999
www.molecularimprints.com

NIL pattern and process dependencies have systematic and random components



Nanoimprinting of spun-on layers exhibits pattern dependencies

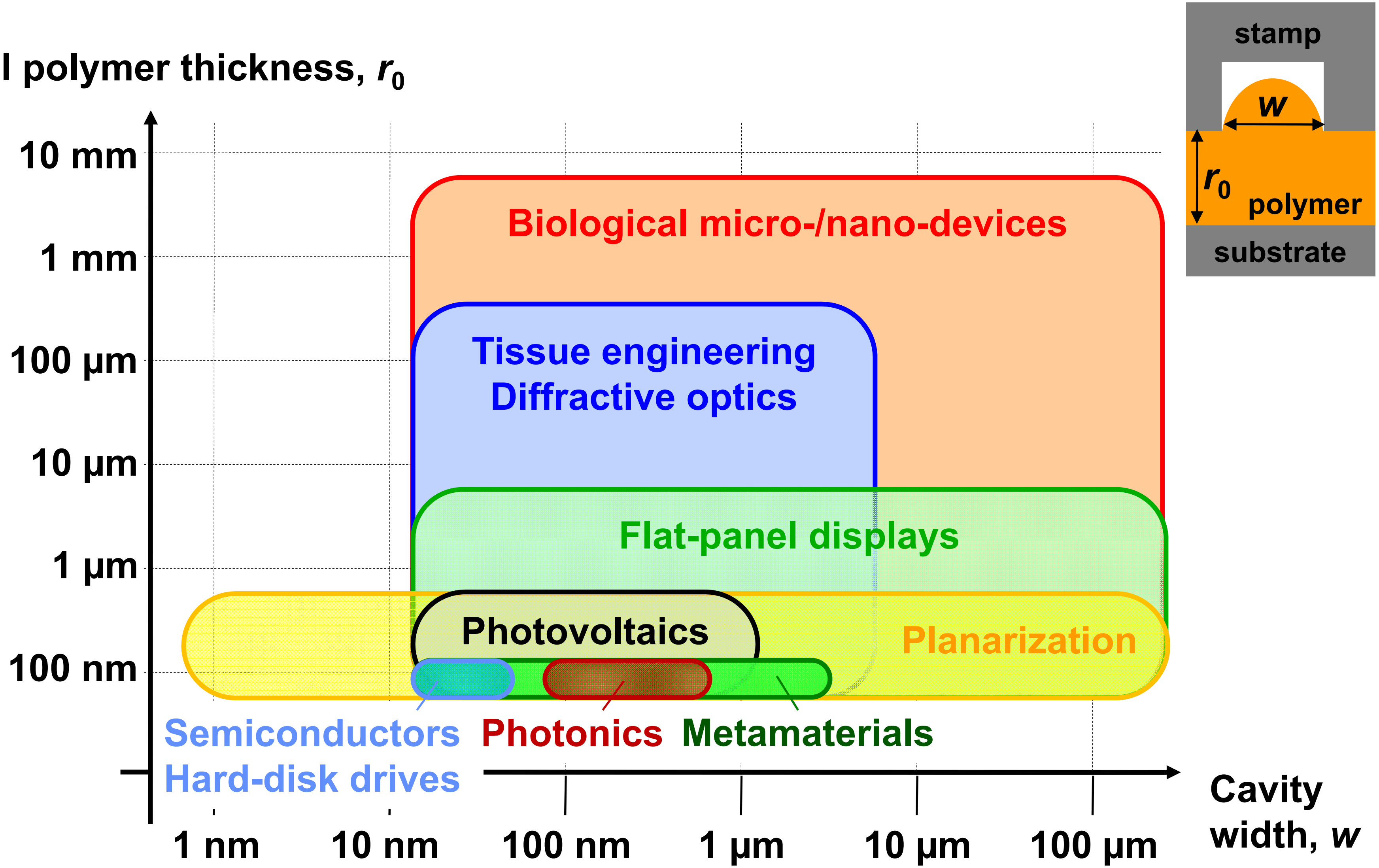


Two relevant timescales for pattern formation:

Local cavity filling

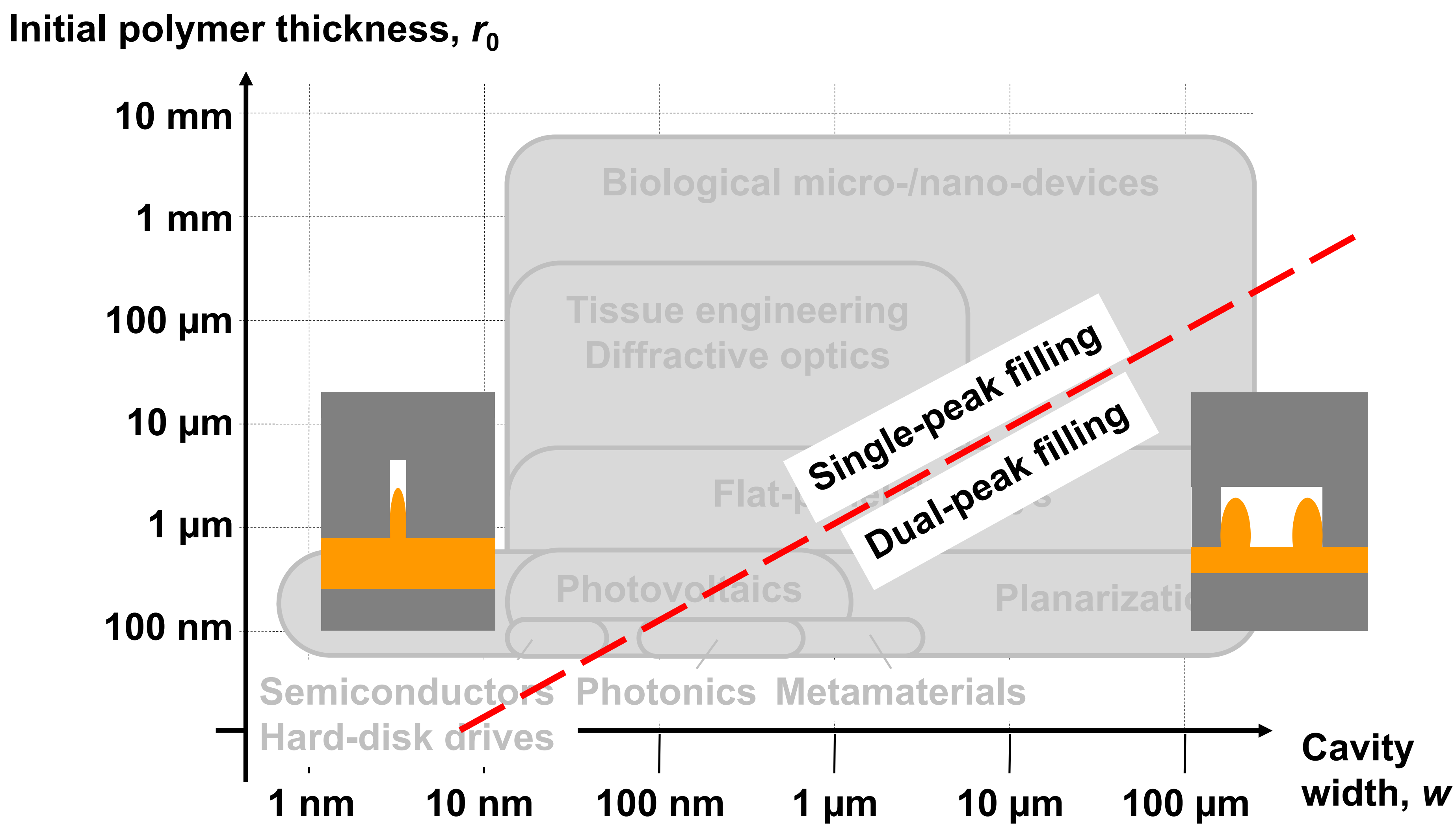
Residual layer thickness (RLT) homogenization

We need a unified simulation approach for micro- and nano-embossing/imprinting



Taylor, NNT 2009

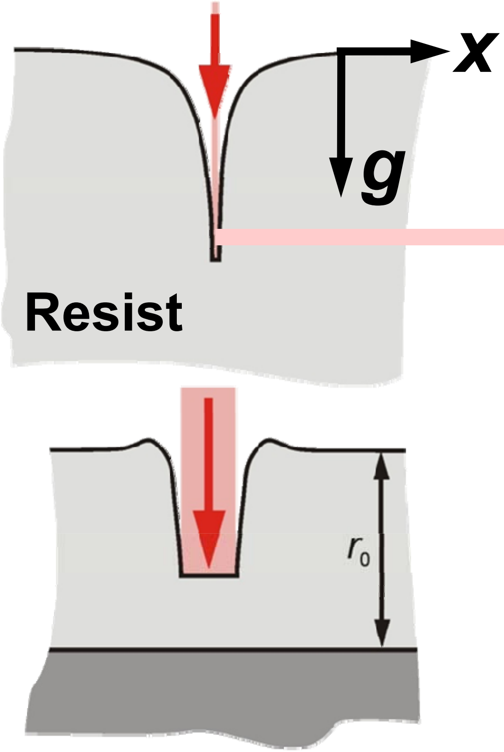
We need a unified simulation approach for micro- and nano-embossing/imprinting



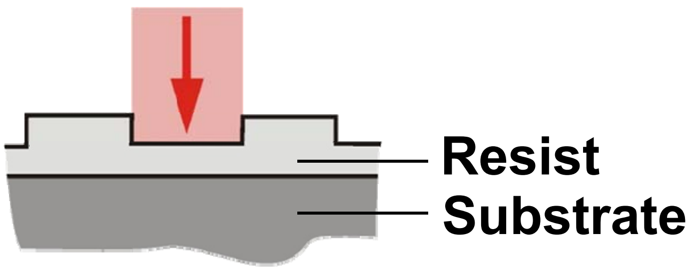
Taylor, NNT 2009

Key: model impulse response $g(x,y,t)$ of resist layer

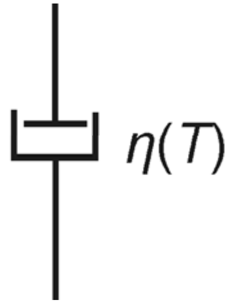
Model in space:



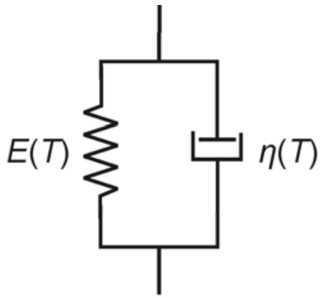
Mechanical impulse applied uniformly over small region at time $t = 0$



Model in time:



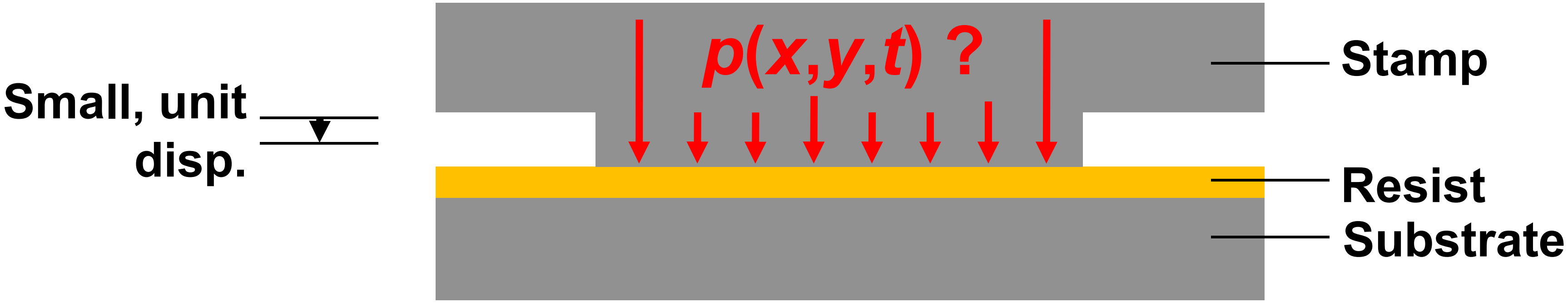
Newtonian: impulse response constant in time for $t > 0$



Viscoelastic: impulse response is function of time.

Taylor, NNT 2009. After Nogi *et al.*, *Trans ASME: J Tribology*, **119** 493-500 (1997)

Change in topography is given by convolution of impulse response with pressure distribution



Time increment

$$\left[p(x,y,t) * g(x,y,t)\right]\Delta t = \mathbf{1}$$

Pressure ?

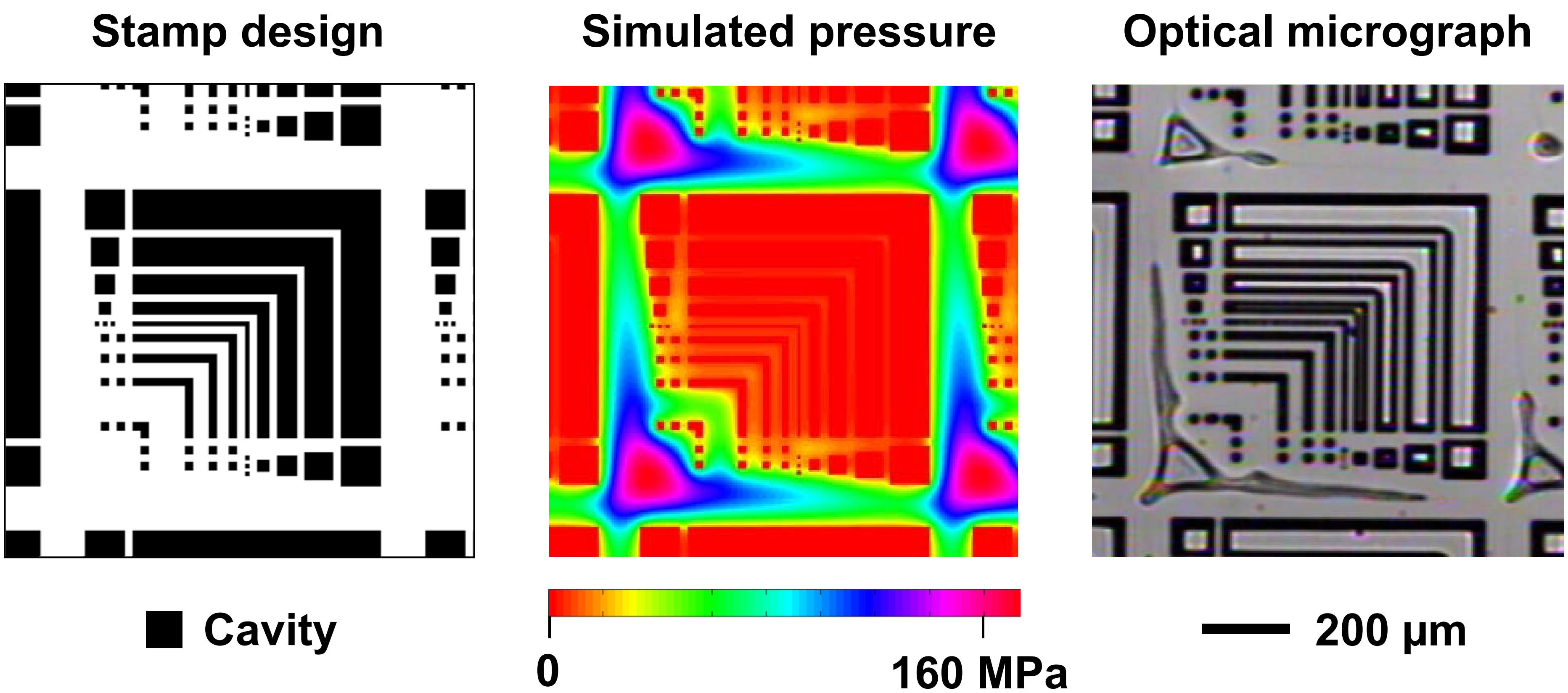
Impulse response

Unit displacement in contact region

Taylor, NNT 2009

Contact pressure distributions can be found for arbitrary stamp geometries

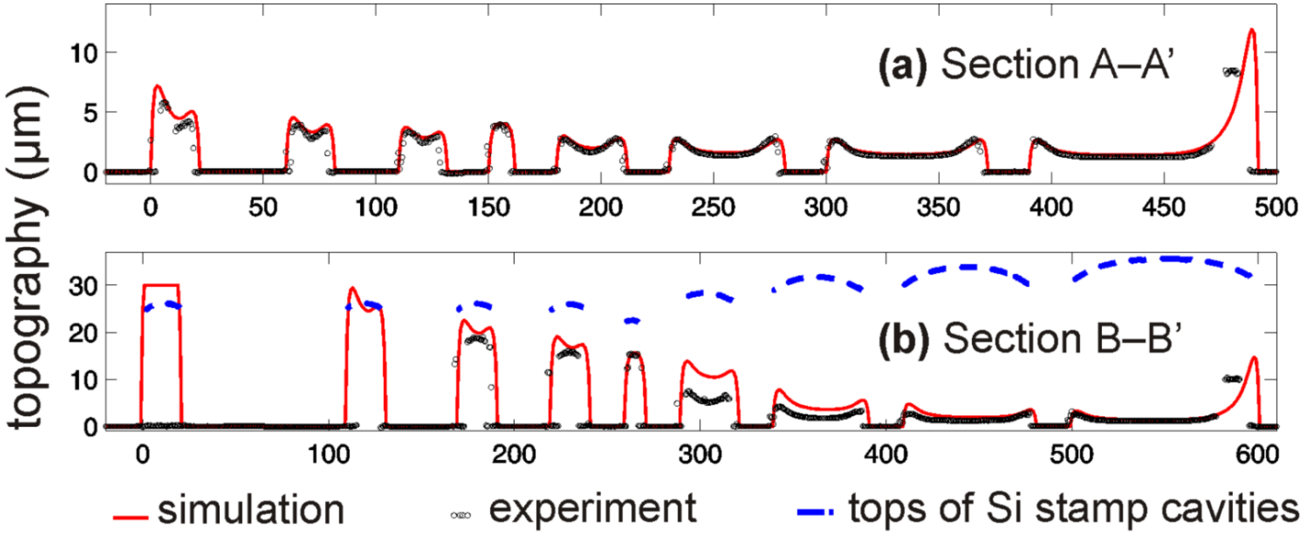
2.3 µm-thick polysulfone film embossed at 205 °C under 30 MPa for 2 mins

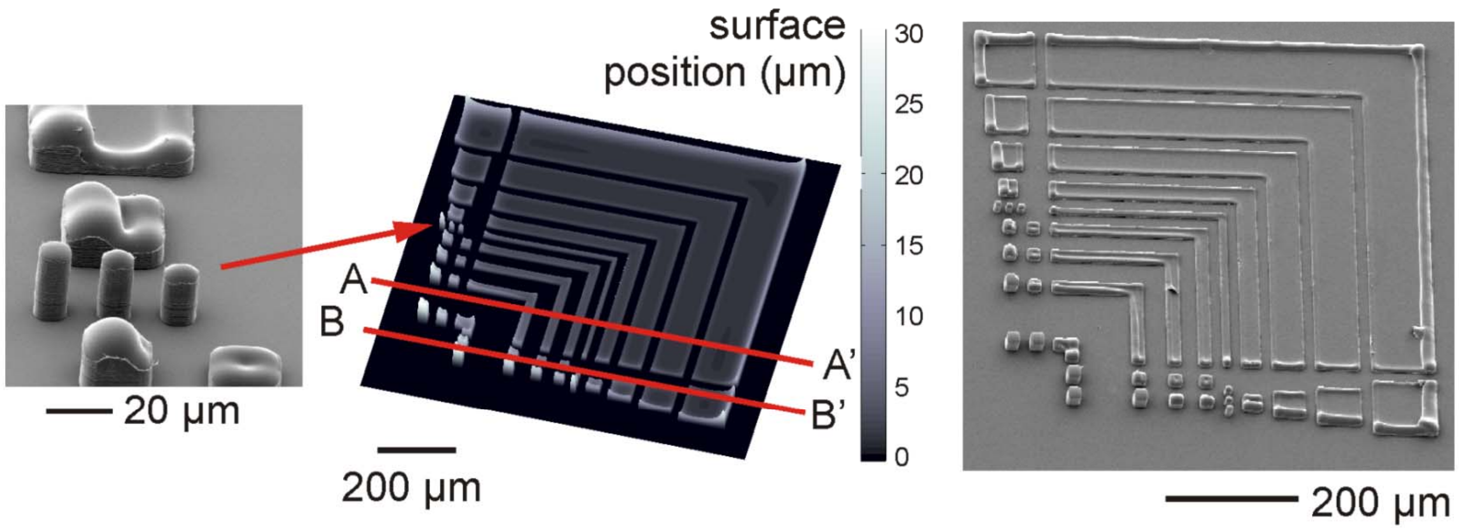


Taylor *et al.*, SPIE 7269 (2009).

Successful modeling of polysulfone imprint

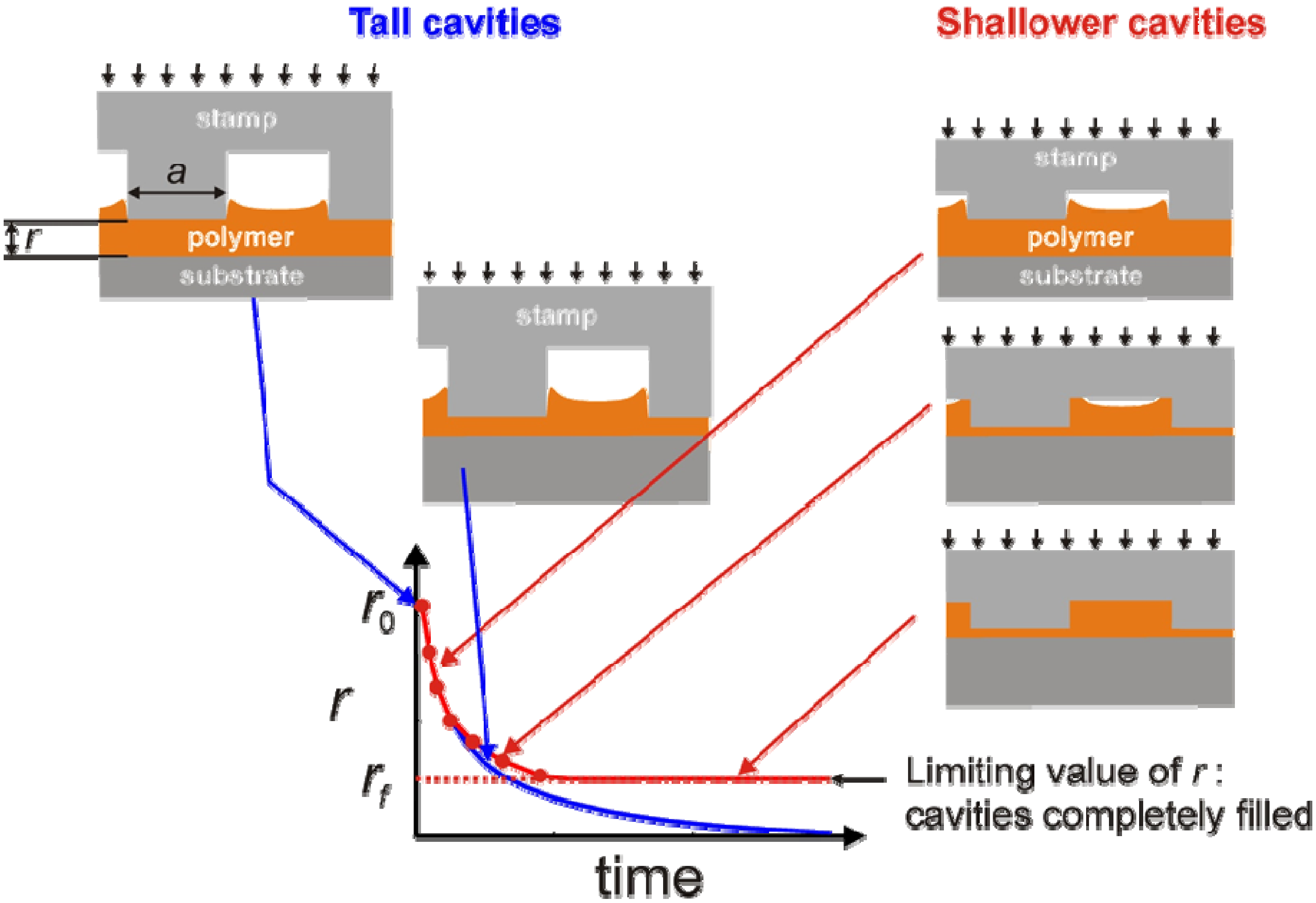
2.3 μm-thick polysulfone film embossed at 205 °C under 30 MPa for 2 mins





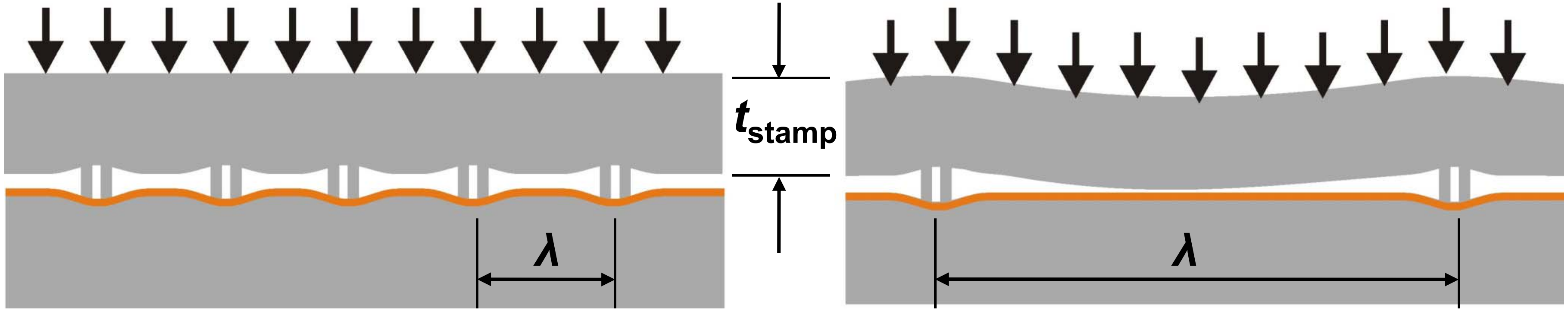
Taylor *et al.*, SPIE 7269 (2009).

Representing layer-thickness reductions

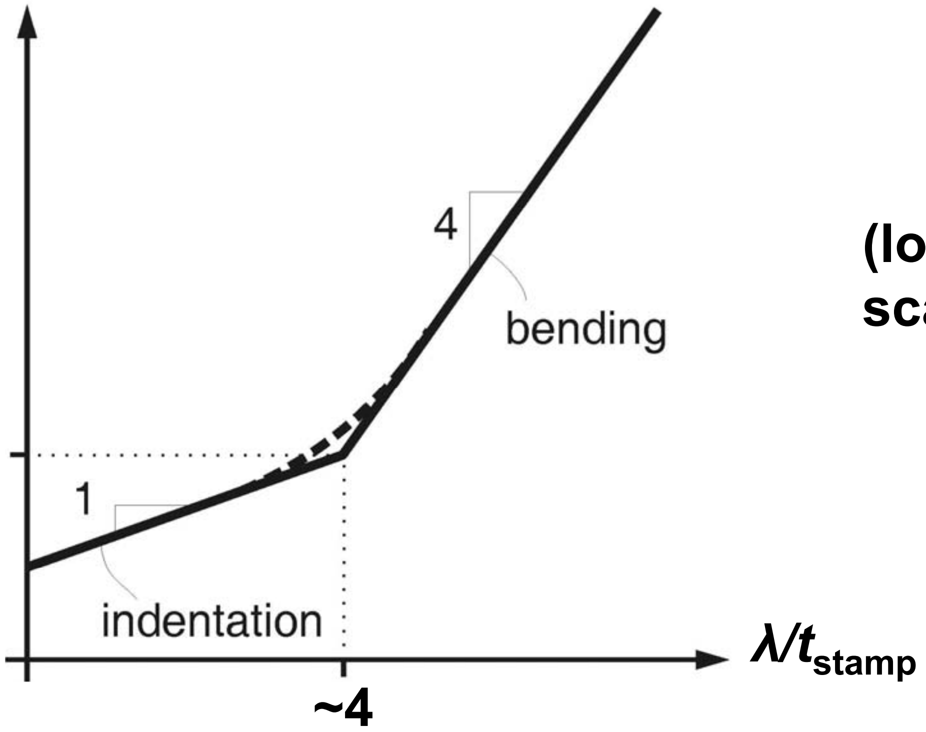


Modeling stamp and substrate deflections

Indentation | **Indentation and bending**



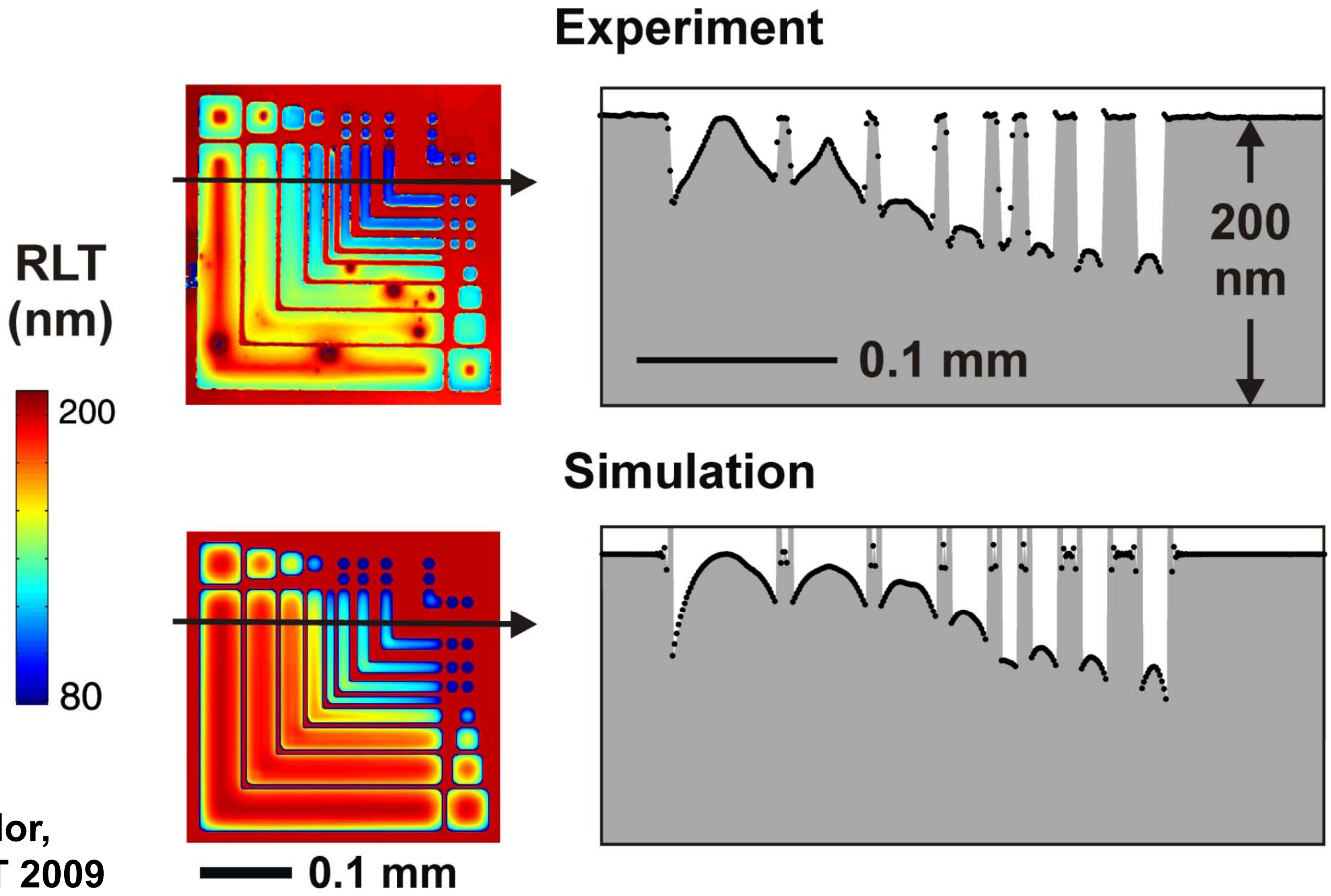
Magnitude of stamp deflection



(log scales)

Simulation method: step-up resist compliance

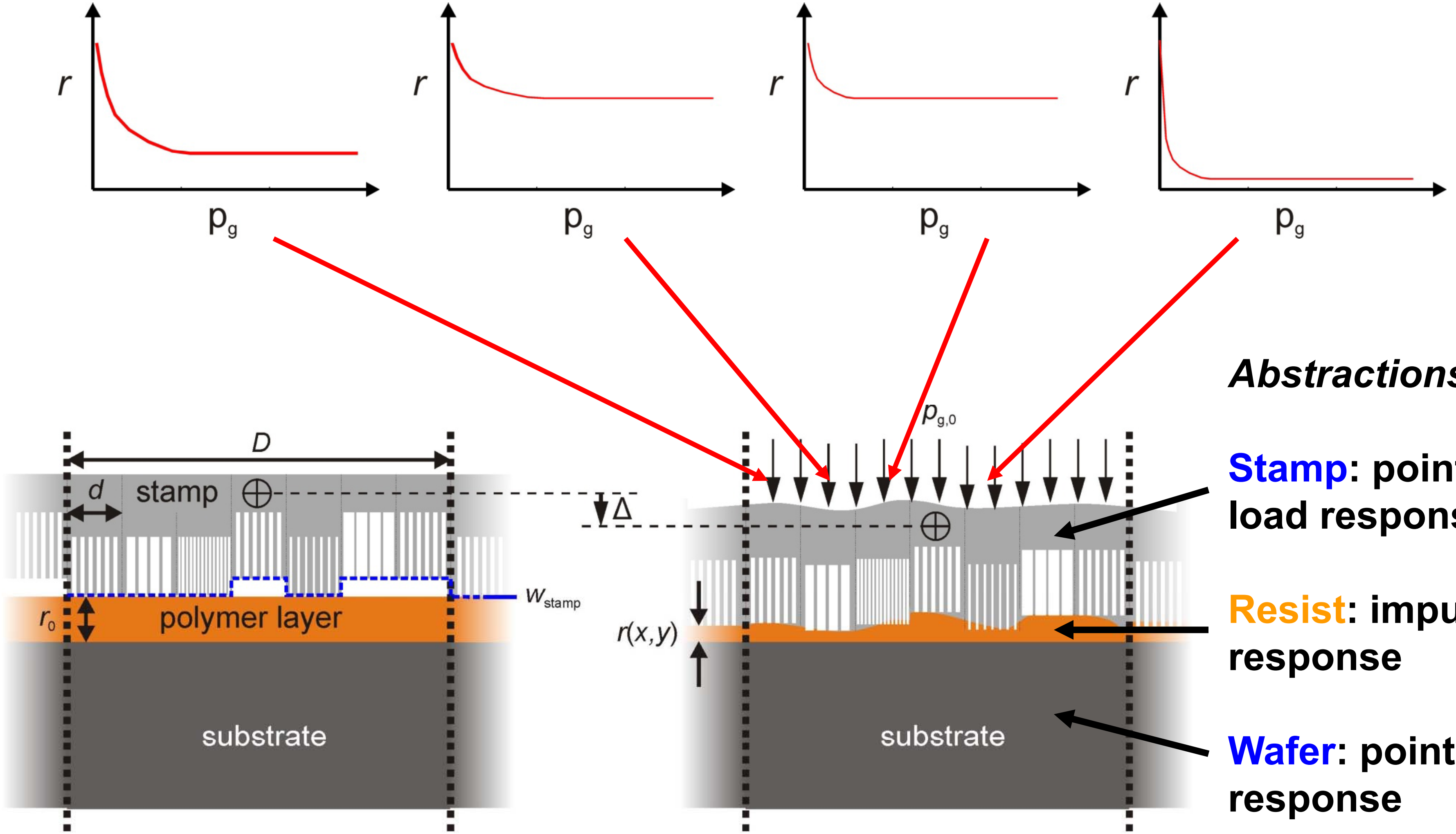
PMMA 495K, *c*. 165 °C, 40 MPa, 1 min



Taylor, NNT 2009

Abstracting a complex pattern

Local relationships between pressure history and RLT:



***Abstractions*:**

Stamp: point-load response

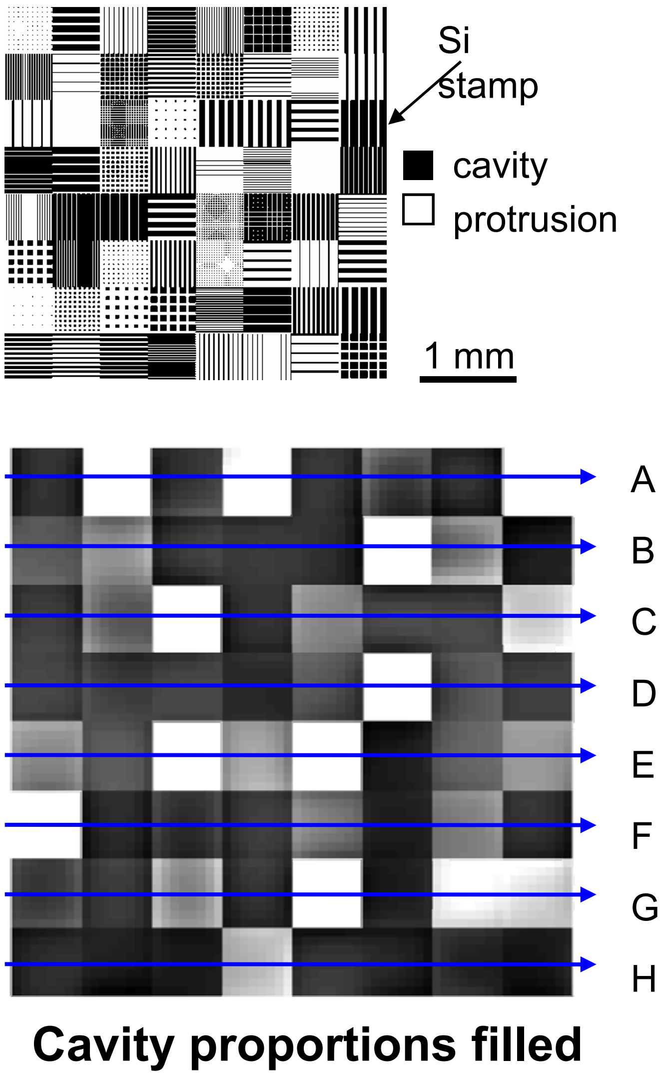
Resist: impulse response

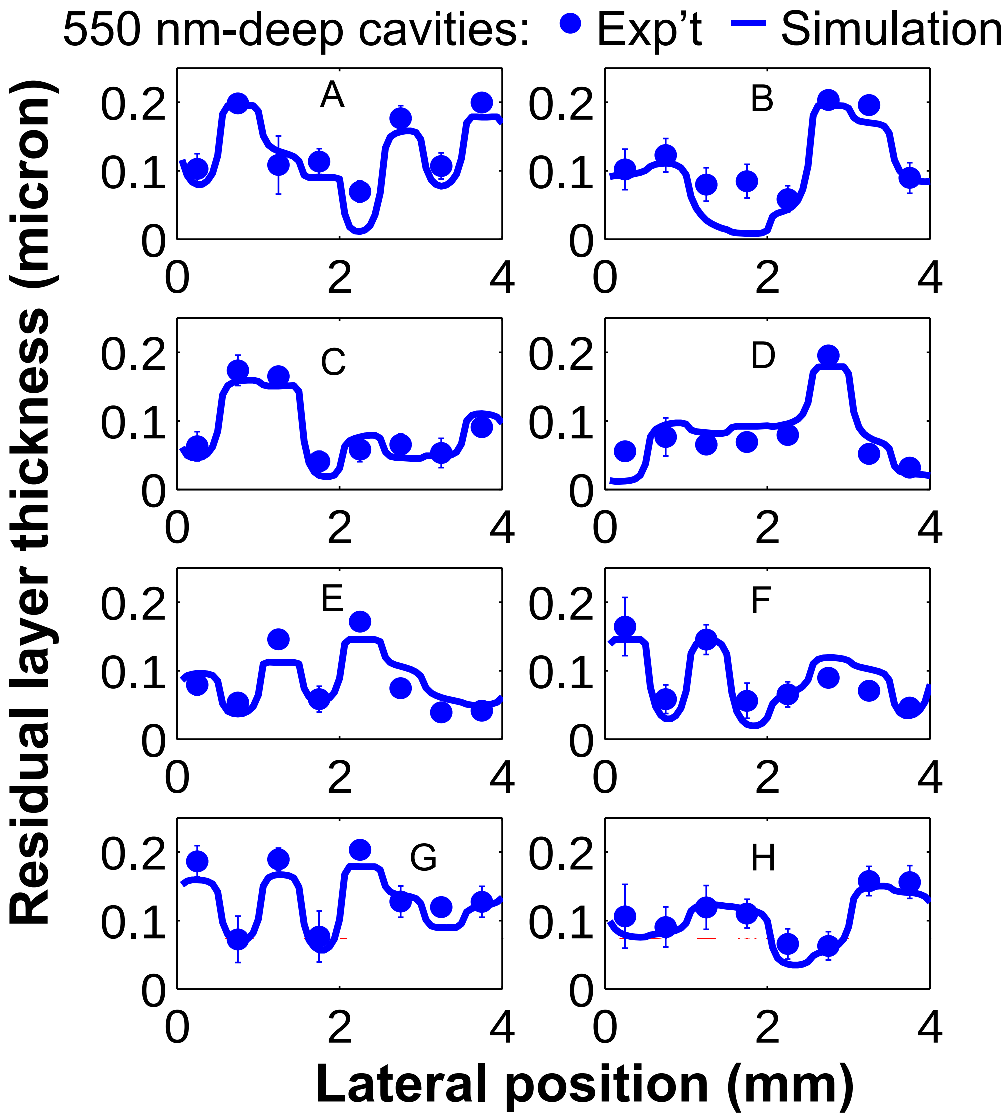
Wafer: point-load response

HK Taylor and DS Boning, NNT 2009; SPIE 7641 (2010)

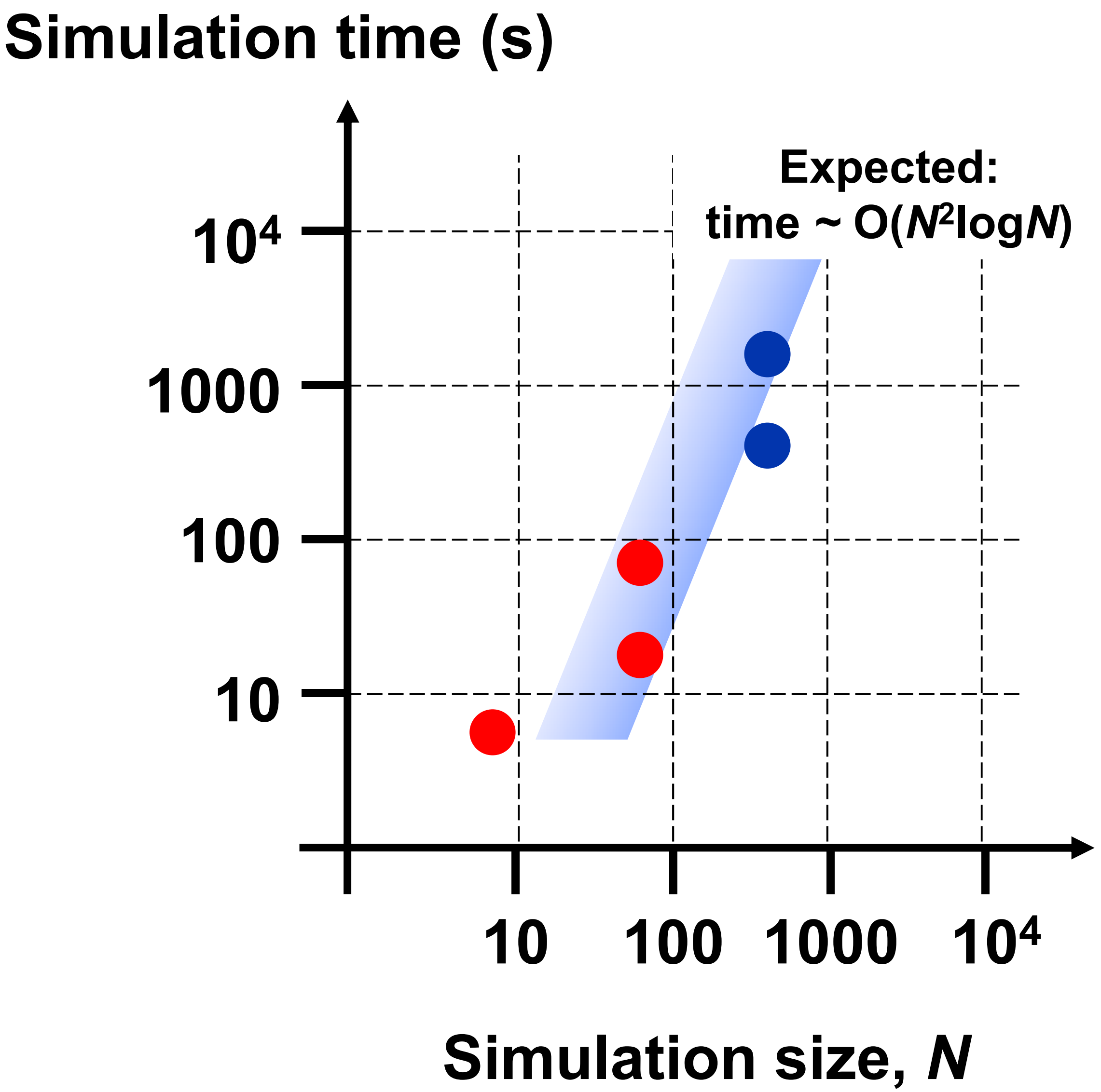
Our NIL simulation technique has been experimentally validated

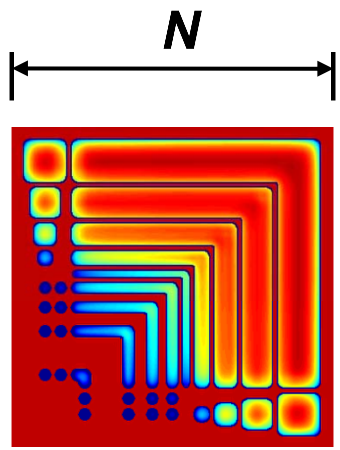
PMMA 495K (200 nm), 180 C, 10 min, 16 MPa, 10 replicates



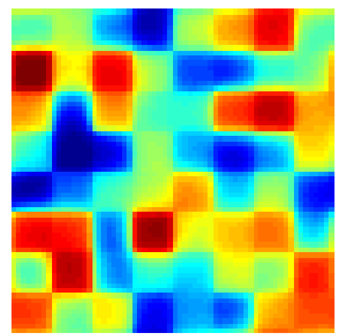


Simulation time





Stamp 1
Feature-scale

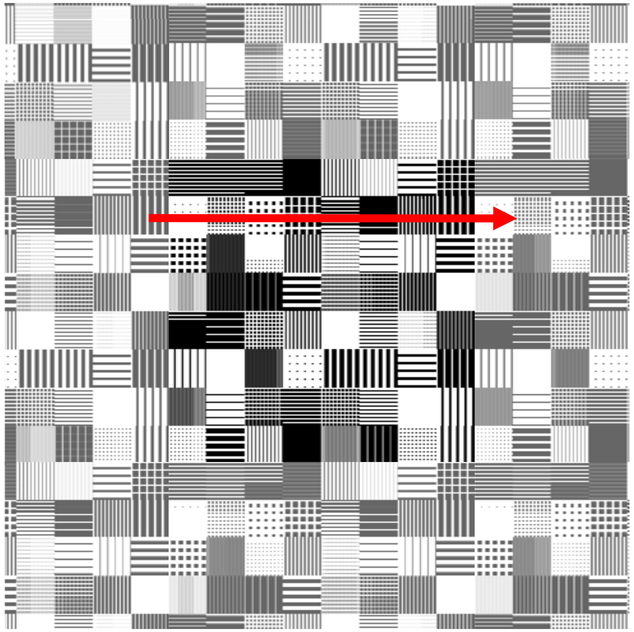


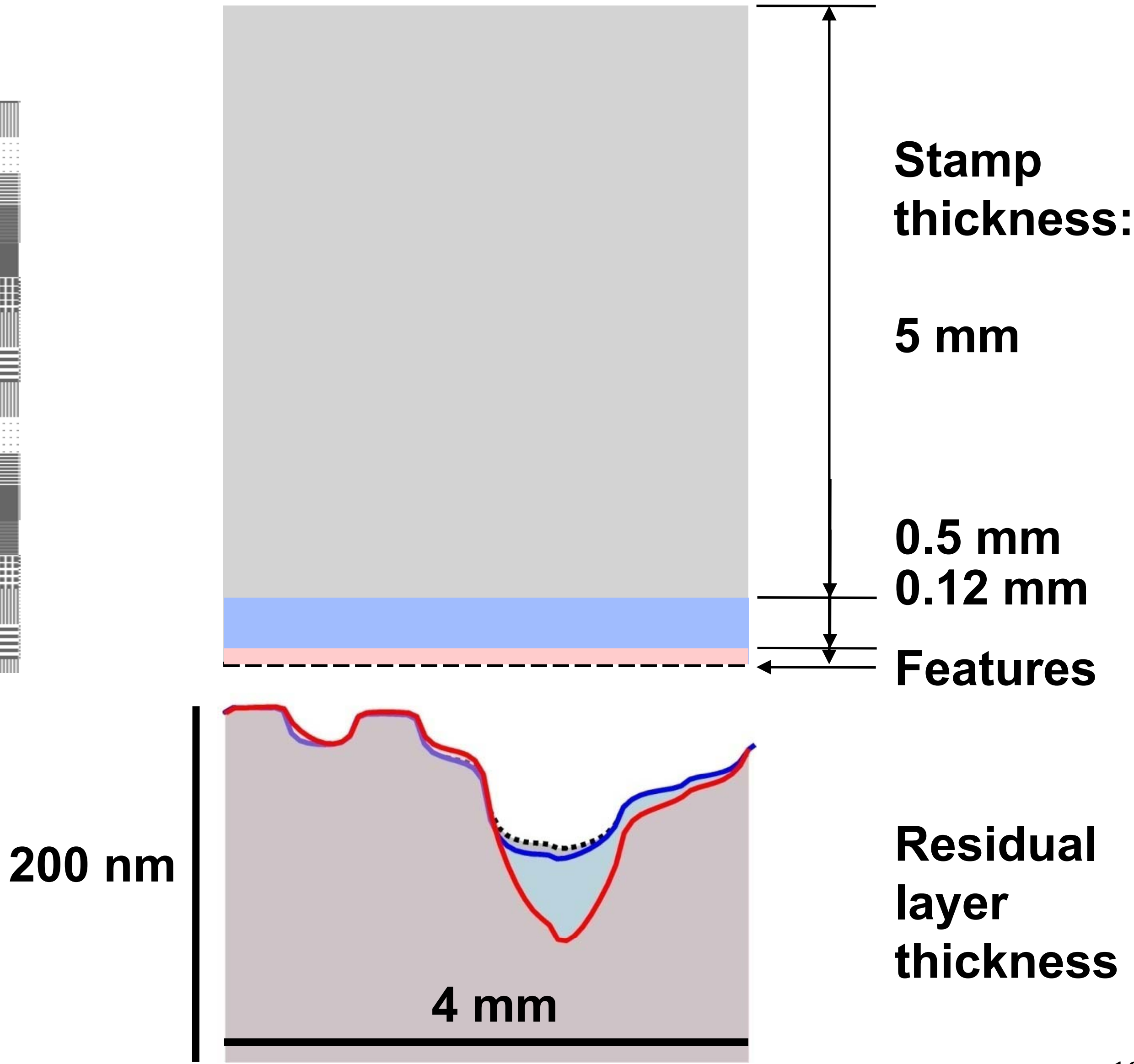
Stamp 2
Abstracted

Strengths of the simulation method

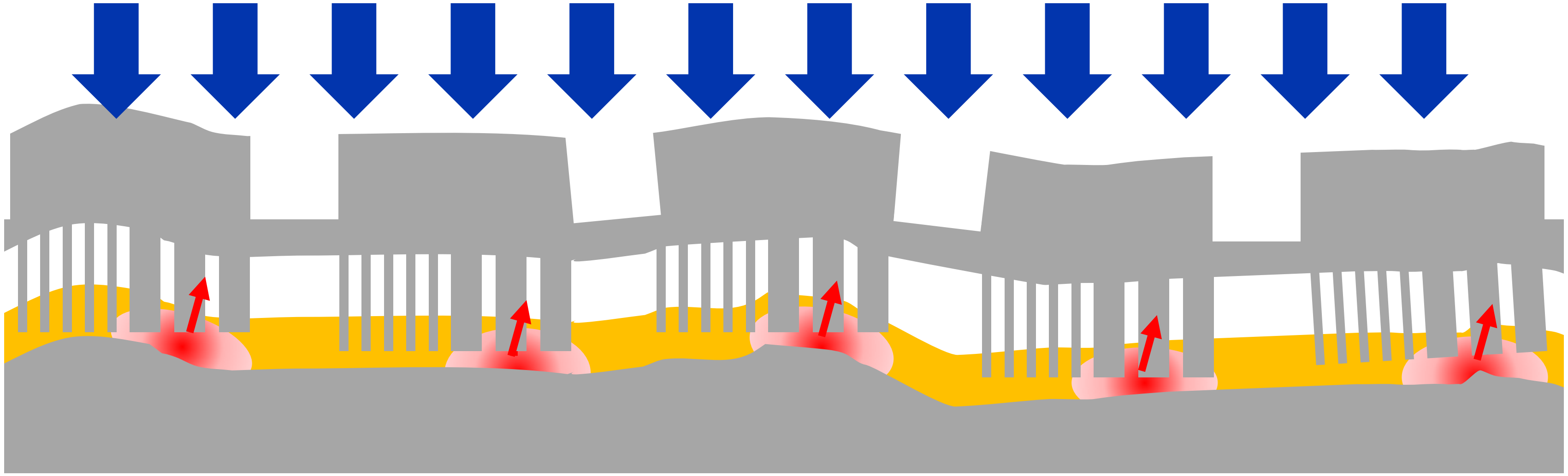
- **A unified simulation approach**
  - Can cope with any layer thickness
  - Can integrate feature sizes ranging over many orders of magnitude
- **Can model any linear viscoelastic material**
- **Speed**
  - At least 1000 times faster than feature-level FEM
- **Implicit periodic boundary conditions are useful**
  - Realistic representation of whole-wafer imprint of many chips
  - Can use edge-padding for non-periodic modeling
- **Suited to quick adaptation for new NIL configurations**
  - Use to explore the use of flexible stamps and substrates
  - Explore the imprinting of non-flat substrates
  - Micro-contact printing; roll-to-roll

Varying stamp's bending stiffness: simulations





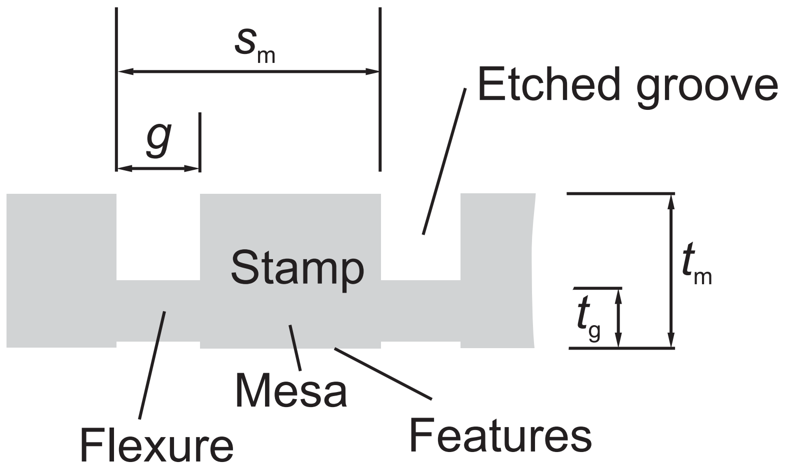
Long-range compliance and short-range rigidity are both desirable in a TNIL stamp

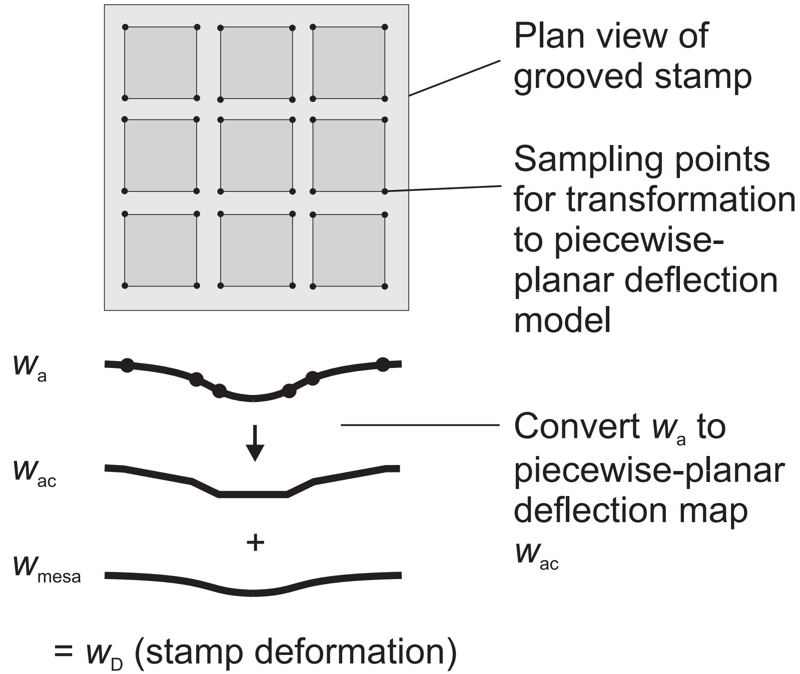


- **Long-range compliance to allow the stamp to conform to random wafer nanotopography**
- **Short-range rigidity to limit systematic pattern dependencies**
- **Making the stamp soft (*i.e.* polymeric) or thin satisfies the first aim but not the second**
- **Structuring the stamp can meet both needs**

Structured stamps provide long-range compliance and short-range rigidity

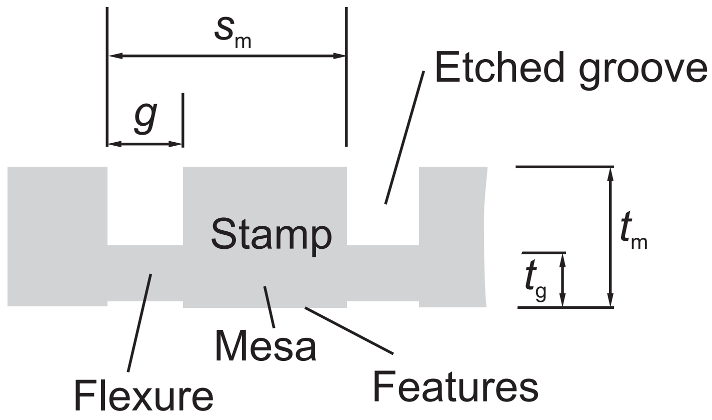
- **A mechanical model of a structured stamp is needed:**
  - **To ensure adequate long-range compliance…**
  - **while keeping fabrication affordable…**
  - **and maximizing the stamp area available for product features.**

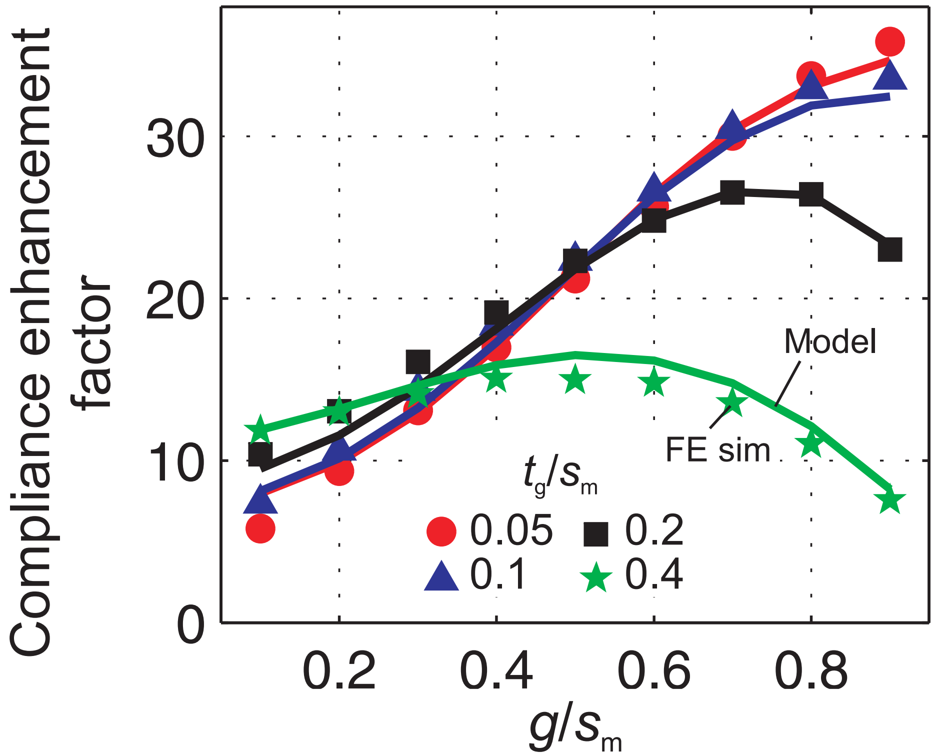




T Nielsen, *et al.*, Proc. 18th IEEE Conf. MEMS 2005, pp. 508–511
HK Taylor, K Smistrup, and DS Boning, MNE 2010

Even a small flexure-gap increases wafer-scale stamp compliance several-fold

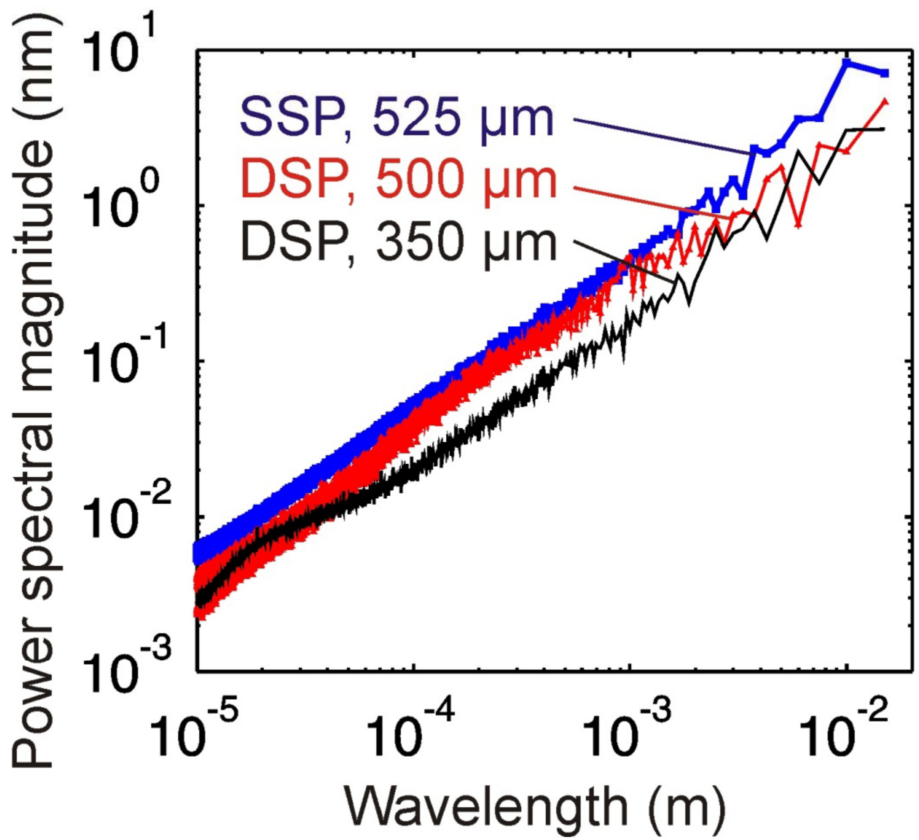




HK Taylor, K Smistrup, and DS Boning, MNE 2010

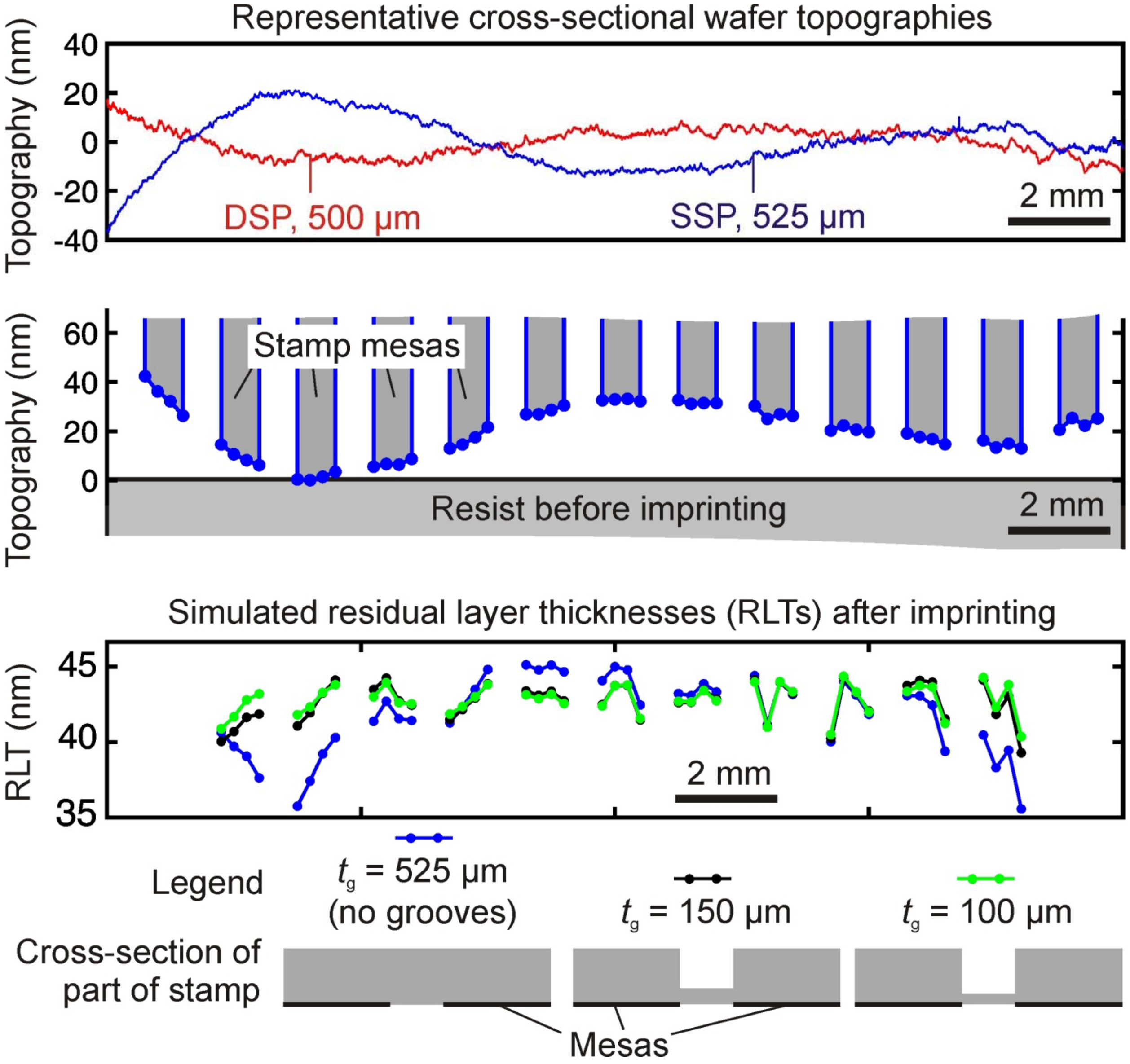
Simulations using a measured wafer topography illustrate long-range compliance

Roughness spectra of three virgin silicon wafers



HK Taylor,
K Smistrup,
and DS Boning,
NNT 2010

Simulations using a measured wafer topography illustrate long-range compliance



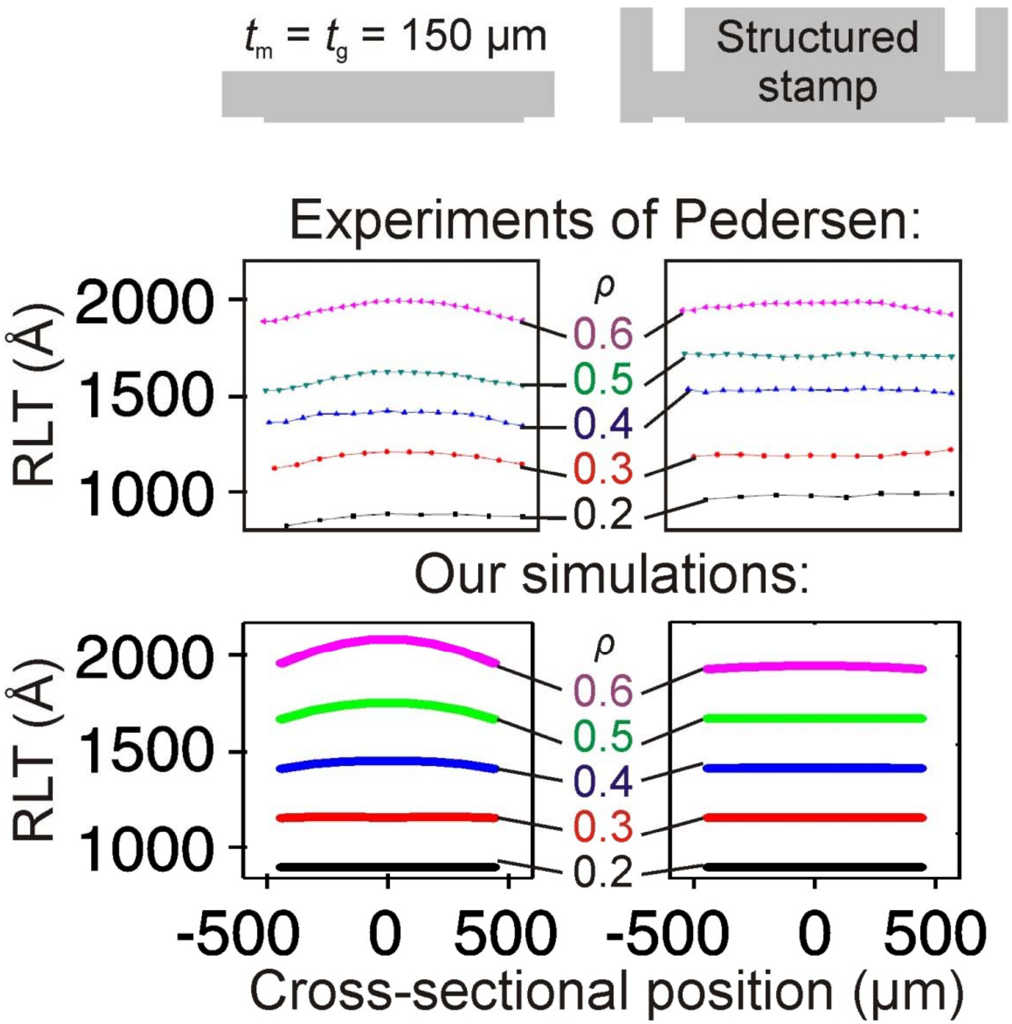
HK Taylor, K Smistrup, and DS Boning, NNT 2010

Simulations using a measured wafer topography illustrate long-range compliance

		Mean *within*-mesa std. dev. (nm)	Mesa-to-mesa std. dev. (nm)
Undeformed stamp topography		1.8	10.4
Simulated RLTs	t_g = 100 µm	1.0	0.3
	t_g = 150 µm	1.1	0.7
	no grooves	1.3	2.3

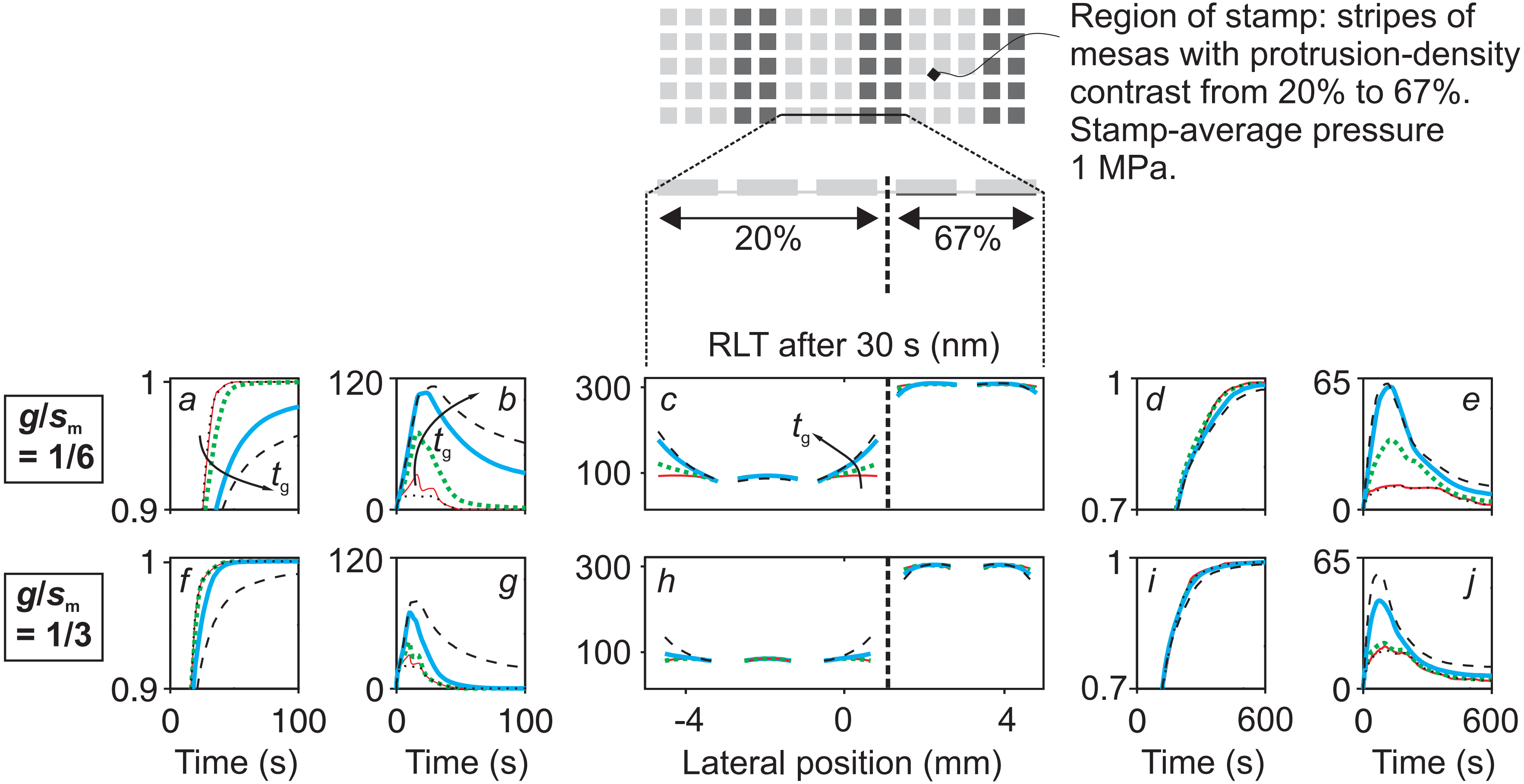
HK Taylor,
K Smistrup,
and DS Boning,
NNT 2010

Die-scale simulations show that structuring the stamp reduces local pattern dependencies



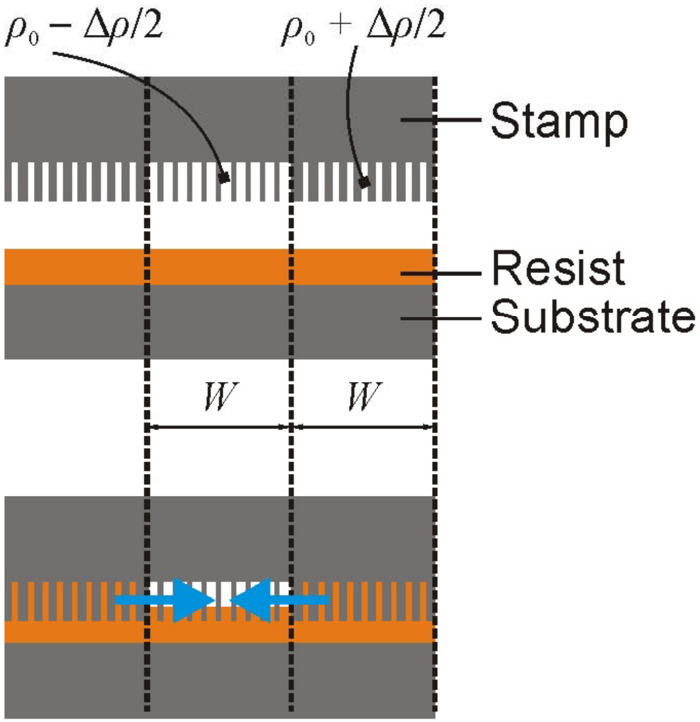
RH Pedersen, *et al.*, *J. Micromech. Microeng.*, vol. 18, p. 055018, 2008.
HK Taylor, K Smistrup, and DS Boning, MNE 2010.

Structured stamps also allow for ‘decoupling’ of differently patterned adjacent mesas



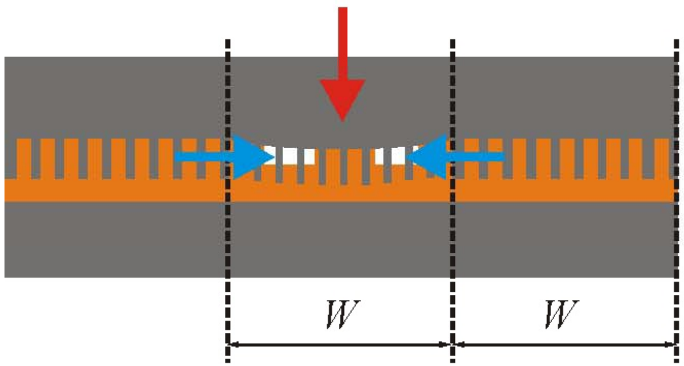
HK Taylor, K Smistrup, and DS Boning, MNE 2010

Cavity-filling time depends on length-scale of pattern-density variation, and stamp stiffness



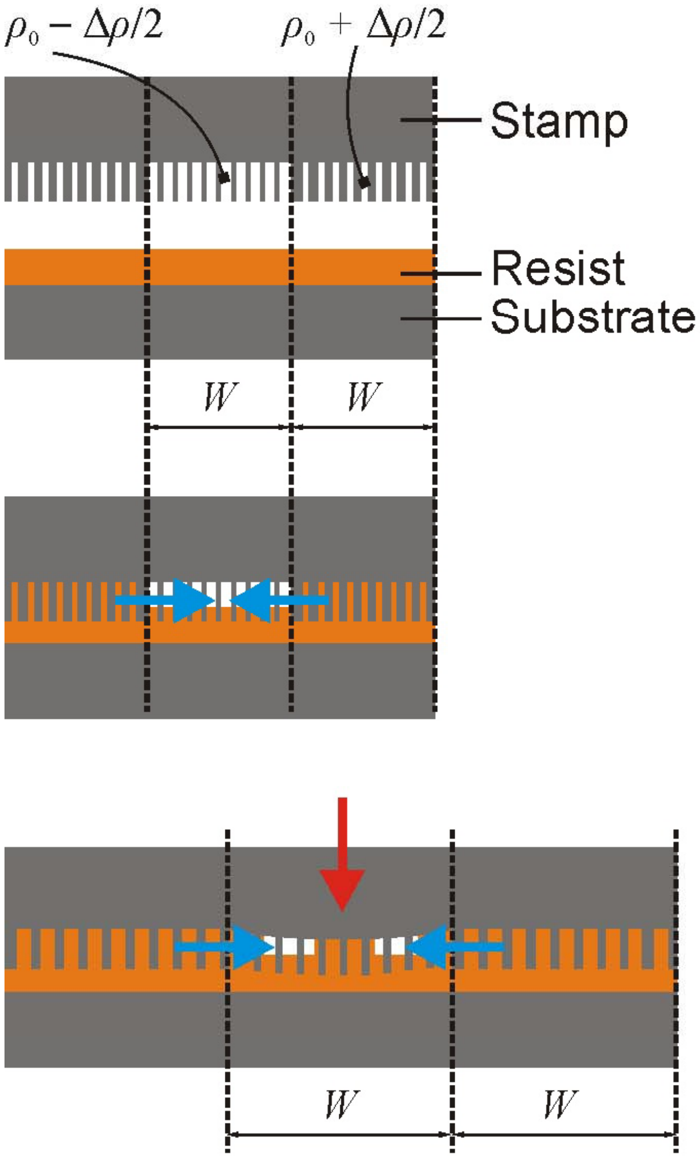
Lower-density region fills by:

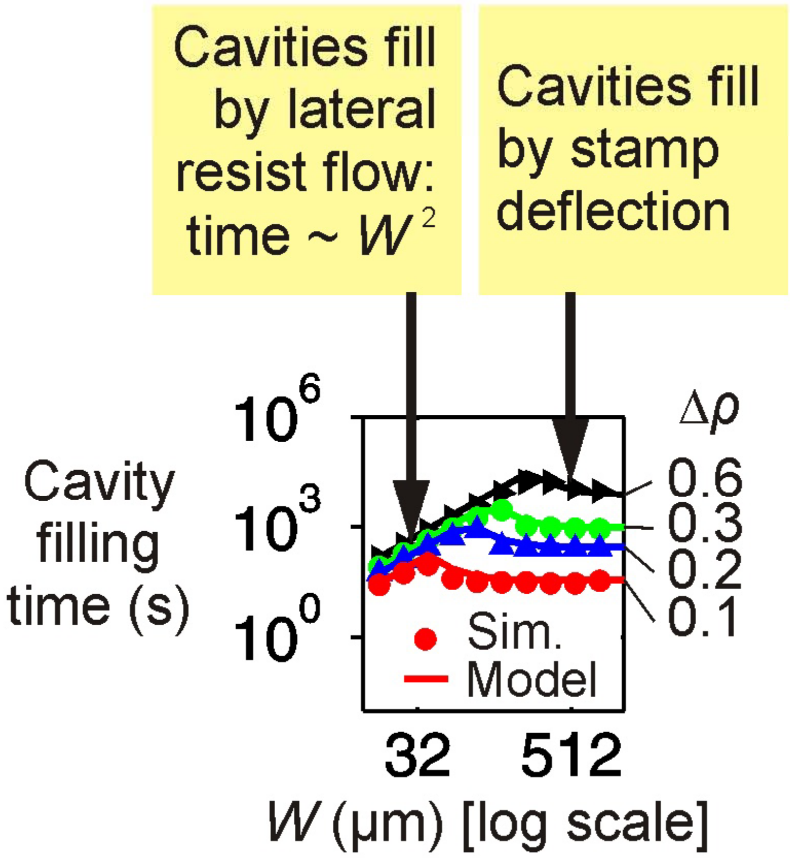
Lateral flow



Lateral flow and stamp deflection

Cavity-filling time depends on length-scale of pattern-density variation, and stamp stiffness

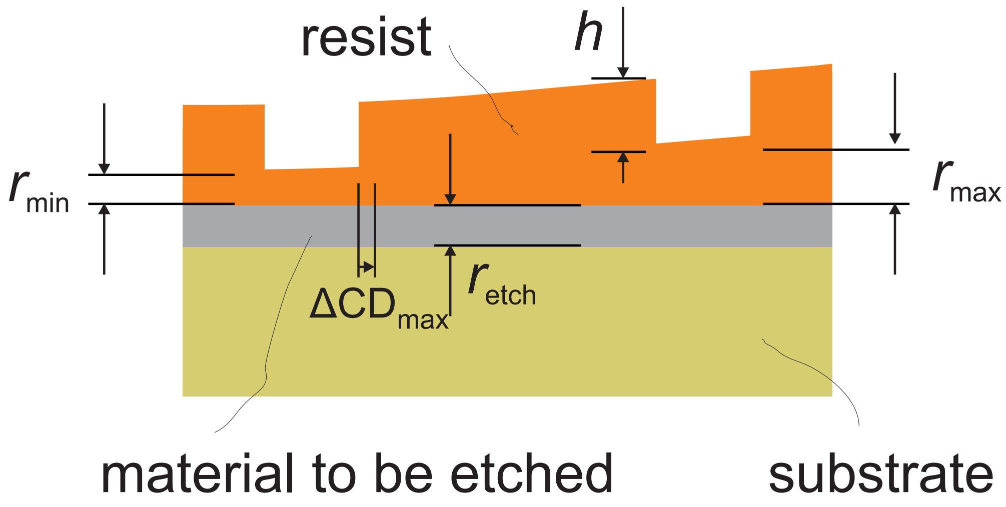




Stamp stiffness: 160GPa (Si)
Resist viscosity: 10^4 Pa.s
Stamp-average pressure: 5 MPa

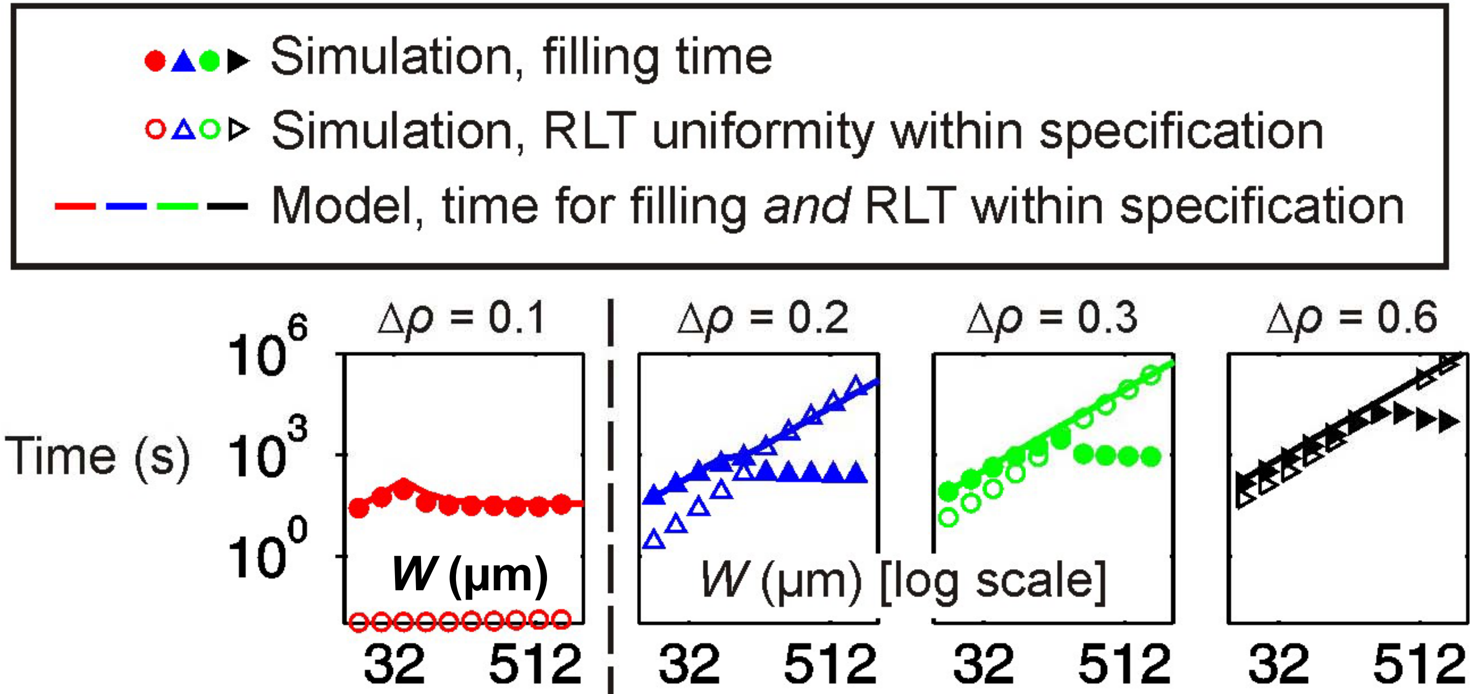
HK Taylor, NNT 2010

If imprinted layer is an etch-mask, RLT specifications depend on resist properties



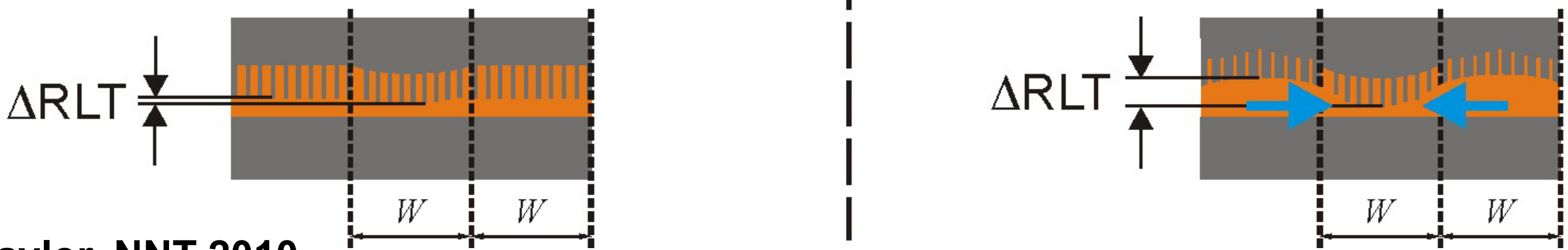
- $(h + r_{max})/r_{max}$ **must be large enough for mask to remain intact throughout etch process**
- **Largest allowable** $r_{max} - r_{min}$ **is likely determined by lateral etch rate and critical dimension specification**

Time to satisfy target for RLT uniformity scales as ~W² for Δρ above a threshold



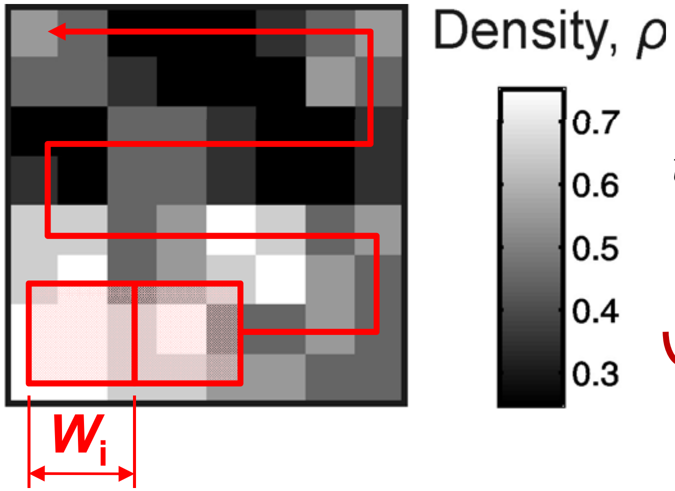
Below a threshold Δρ
(0.17 for these assumptions)
RLT within spec as soon as cavities filled

For larger Δρ
Lateral resist flow needed after filling



HK Taylor, NNT 2010

We postulate a cost function to drive the insertion of dummy fill into rich designs

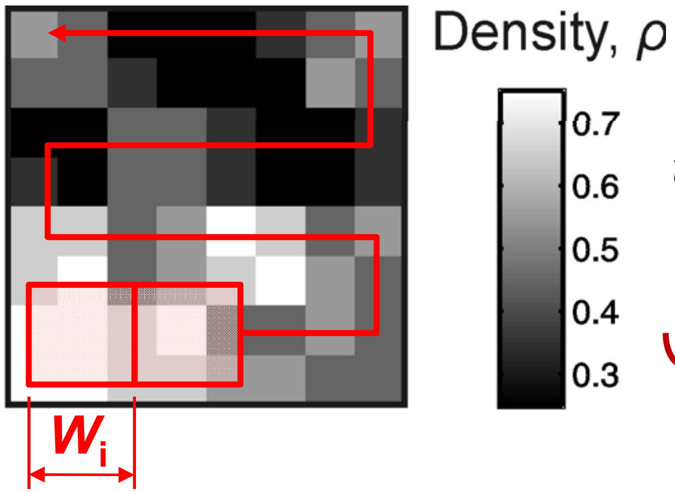


$$\hat{t}_{fill} = \sum_{i=0}^{N} \frac{W_i^{\,2}\eta}{16 p_0} \left[\frac{1}{\left[r_0 - h\left(1-\rho_0\right)\right]^2} - \frac{1}{\left[r_0 - h\left(1-\rho_0 - \frac{\Delta\rho_i}{2}\right)\right]^2} \right]$$

- **Abutting windows of size W_i swept over design**
- **$\Delta\rho_i$ is maximal density contrast between abutting windows in any location**
- **Objective is to minimize sum of contributions from N+1 window sizes**

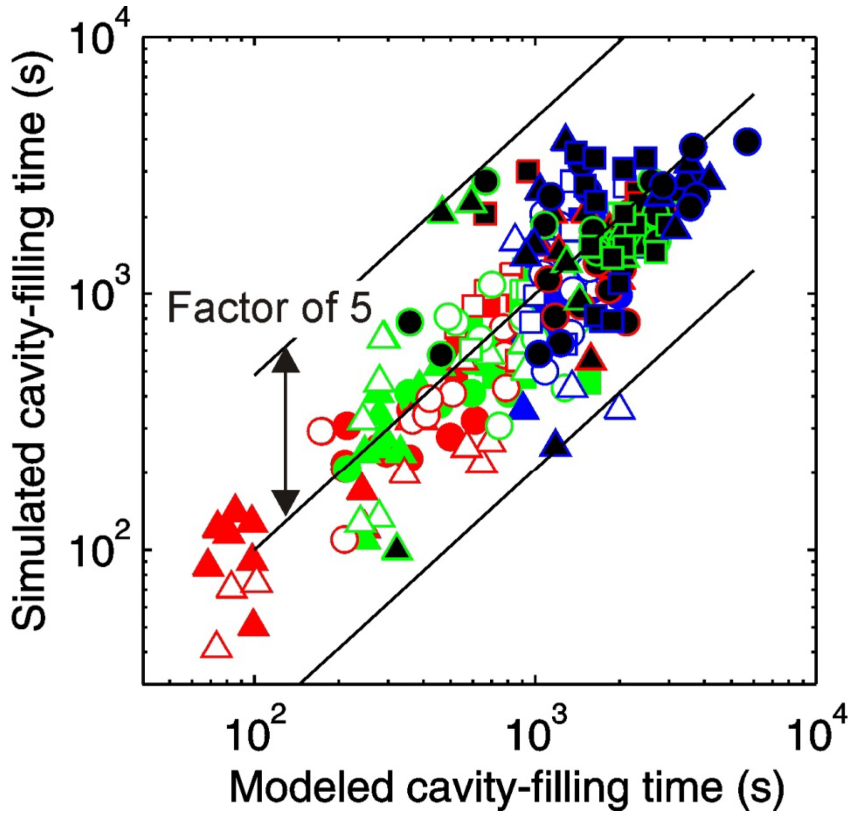
- **h: protrusion height on stamp**
- **r_0: initial resist thickness**

We postulate a cost function to drive the insertion of dummy fill into rich designs



$$\hat{t}_{fill} = \sum_{i=0}^{N} \frac{W_i^2 \eta}{16 p_0} \left[\frac{1}{\left[r_0 - h\left(1-\rho_0\right)\right]^2} - \frac{1}{\left[r_0 - h\left(1-\rho_0 - \frac{\Delta\rho_i}{2}\right)\right]^2} \right]$$

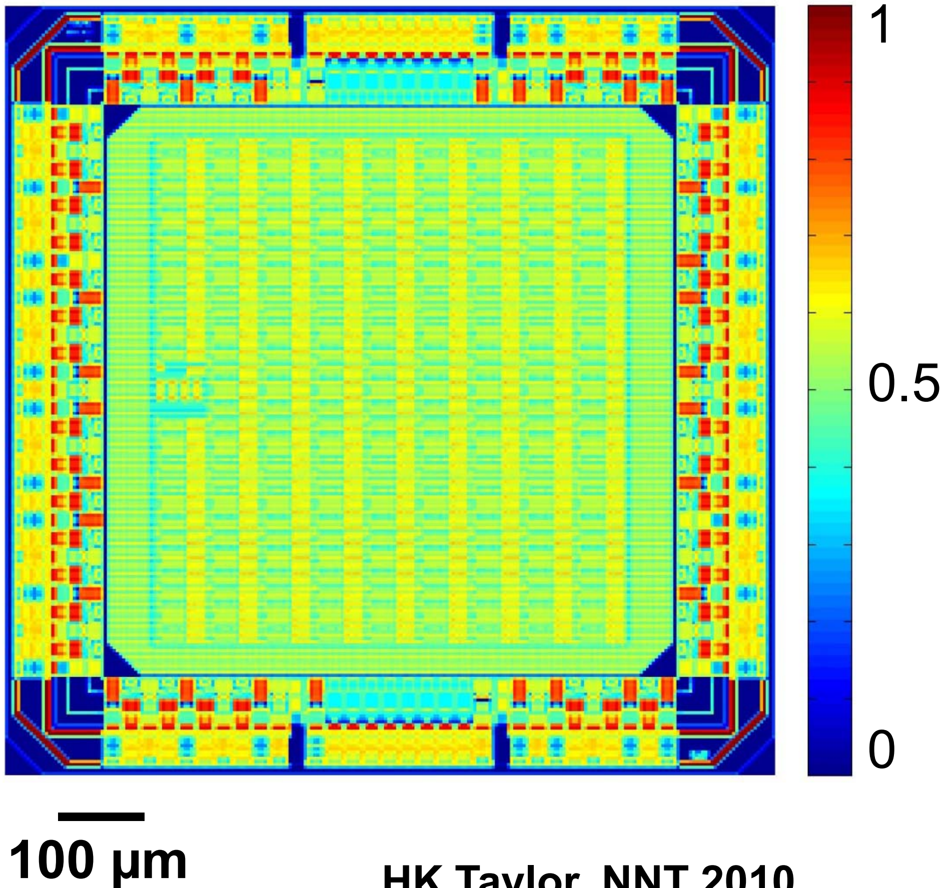
Δρ:	0.05	0.1	0.2
W_i = 32 μm	▲	●	■
(Distinguished by symbol shape)			
W_i = 64 μm	△ (red outline)	△ (green outline)	△ (blue outline)
(Distinguished by outline color)			
W_i = 128 μm	▲ (red fill)	△ (white fill)	▲ (black fill)
(Distinguished by fill color)			



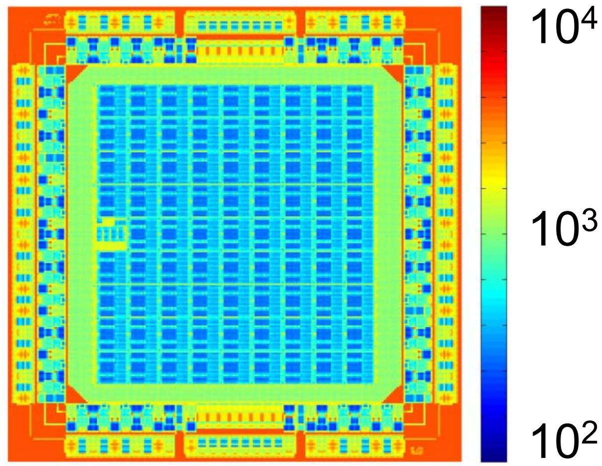
A simple density-homogenization scheme offers faster filling and more uniform RLT

Metal 1 of example integrated circuit: min. feature size 45 nm

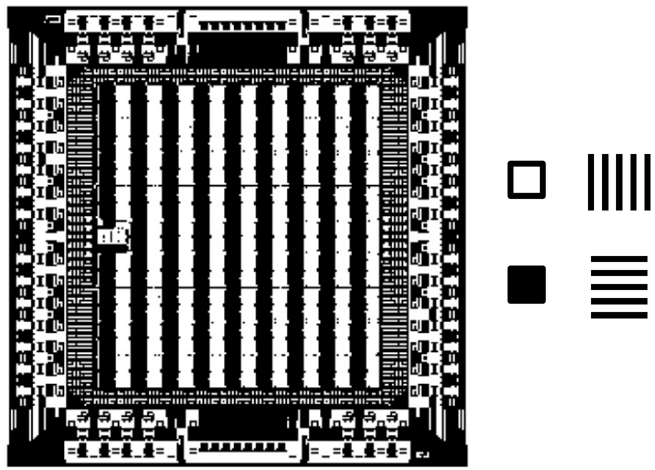
Stamp protrusion pattern density: *without* dummy fill



Characteristic feature pitch (nm)

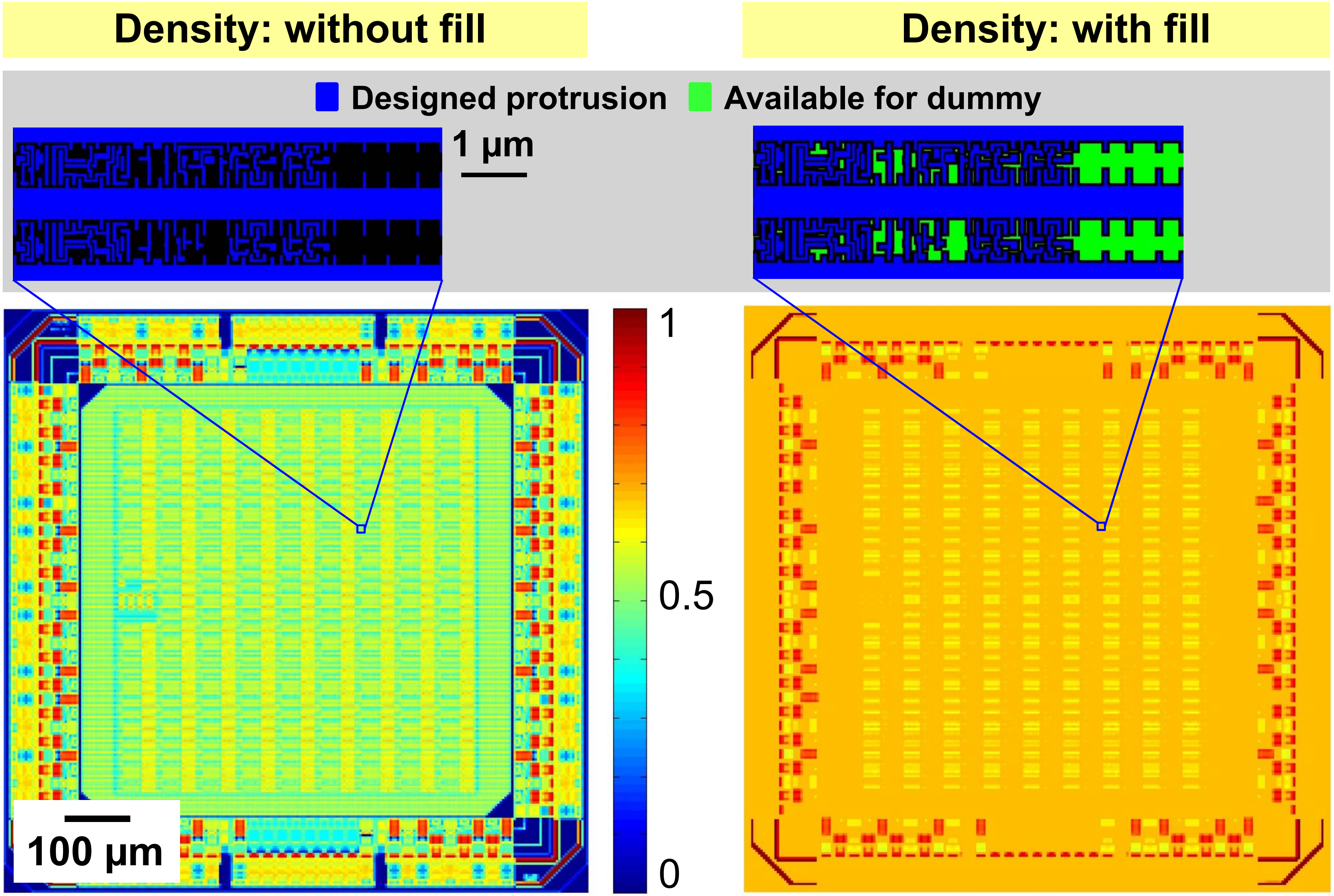


Predominant feature orientation

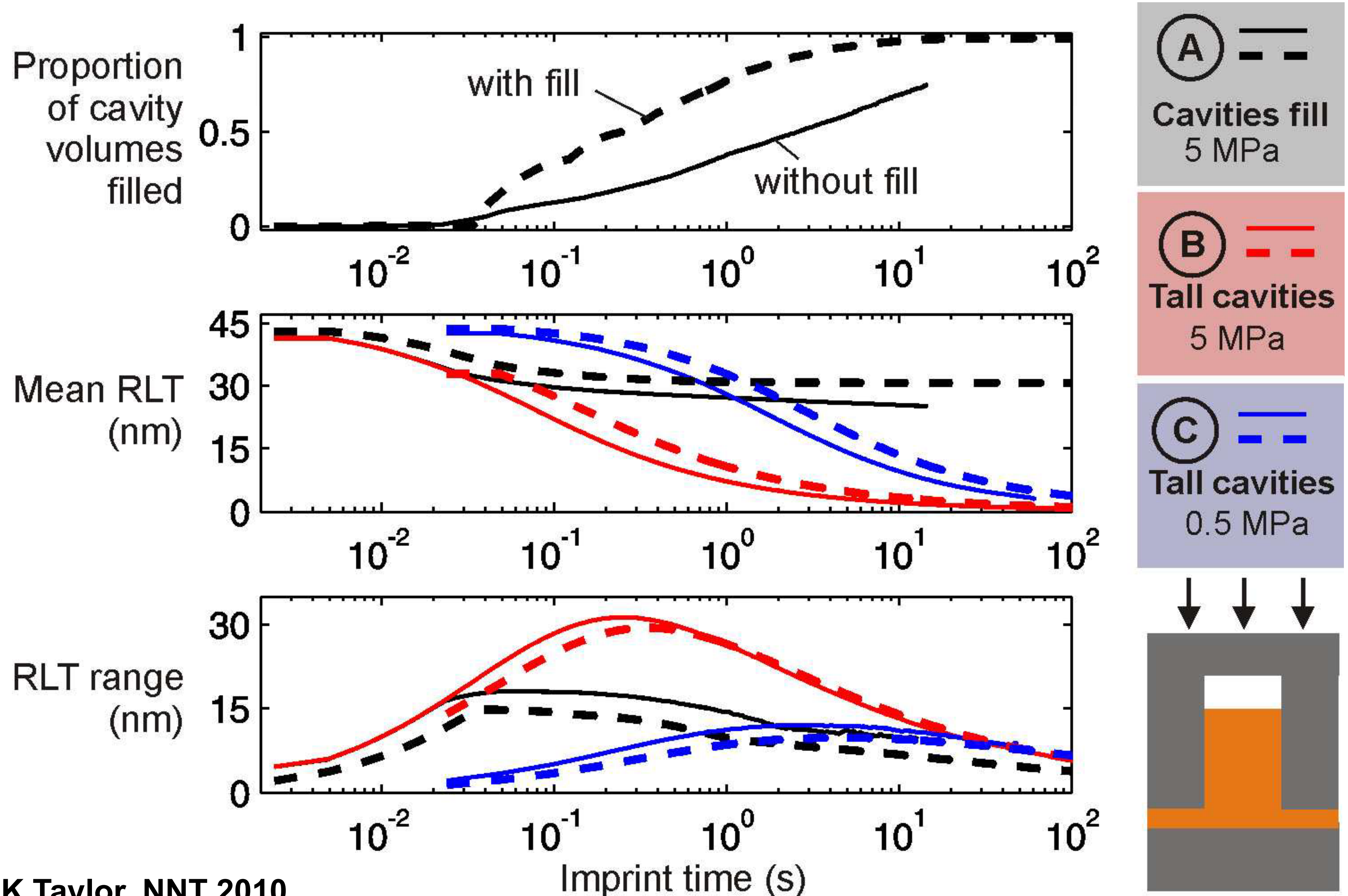


HK Taylor, NNT 2010

A simple density-homogenization scheme offers faster filling and more uniform RLT

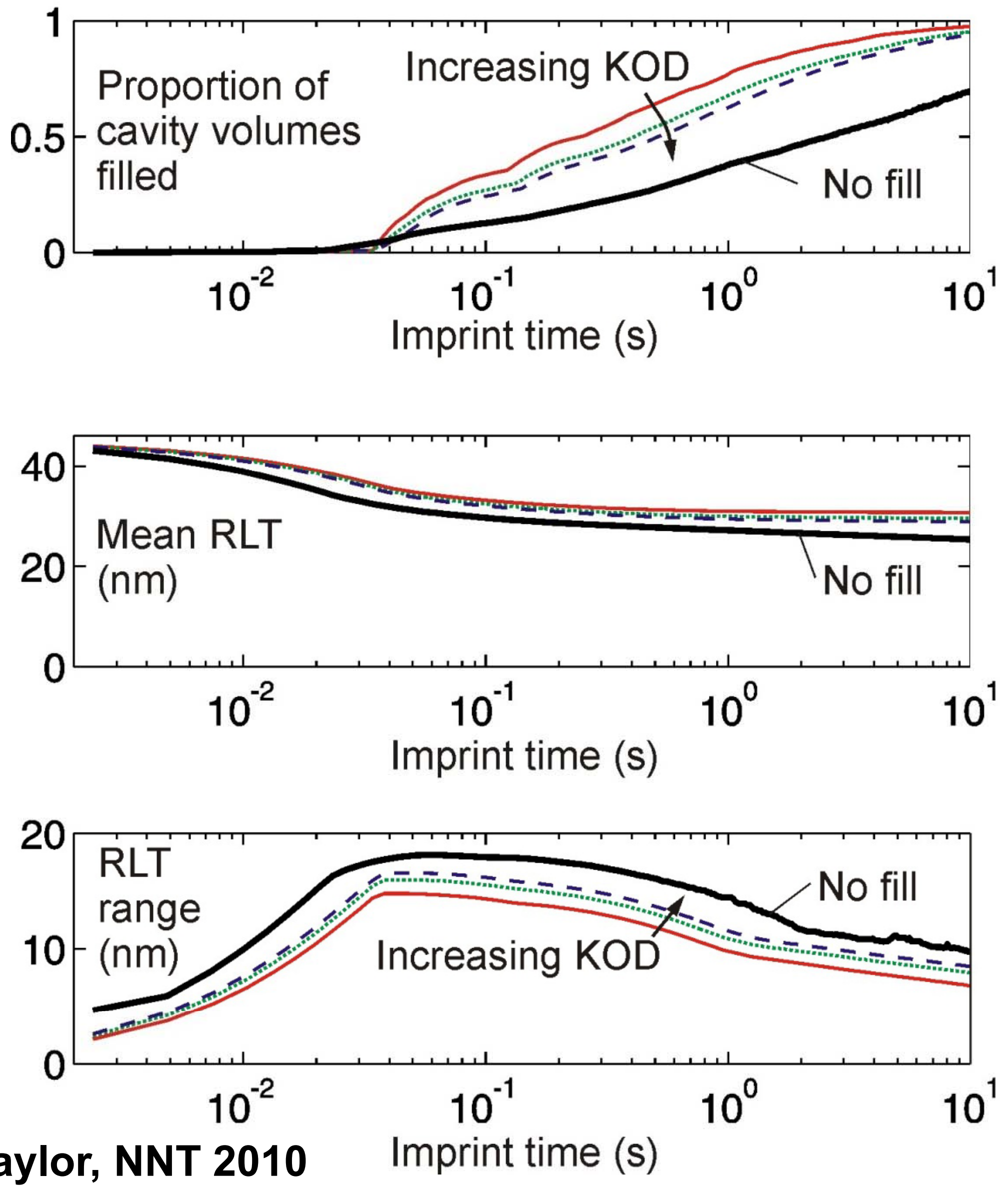


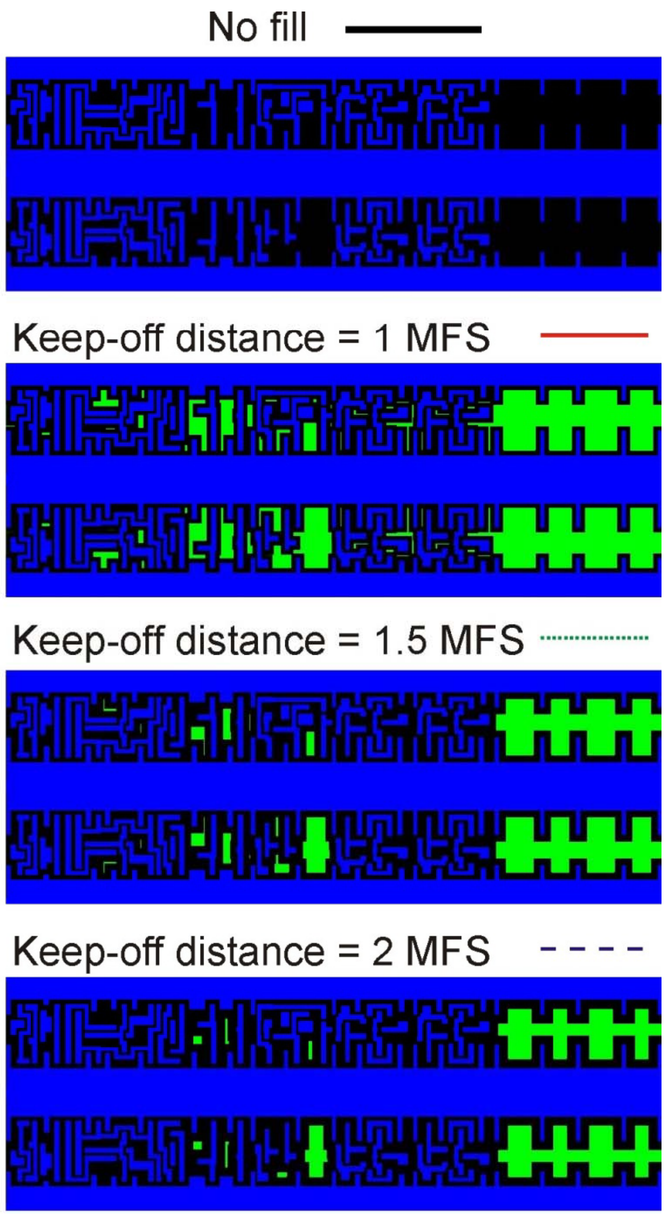
If stamp cavities do not fill, smaller RLTs are possible but RLT may be less uniform



HK Taylor, NNT 2010

Increasing 'keep-off' distance may reduce IC parasitics, but degrades RLT performance





HK Taylor, NNT 2010

Summary: modeling and mitigation of process and pattern dependencies in NIL