

# Towards nanoimprint lithography-aware layout design checking

25 February 2010

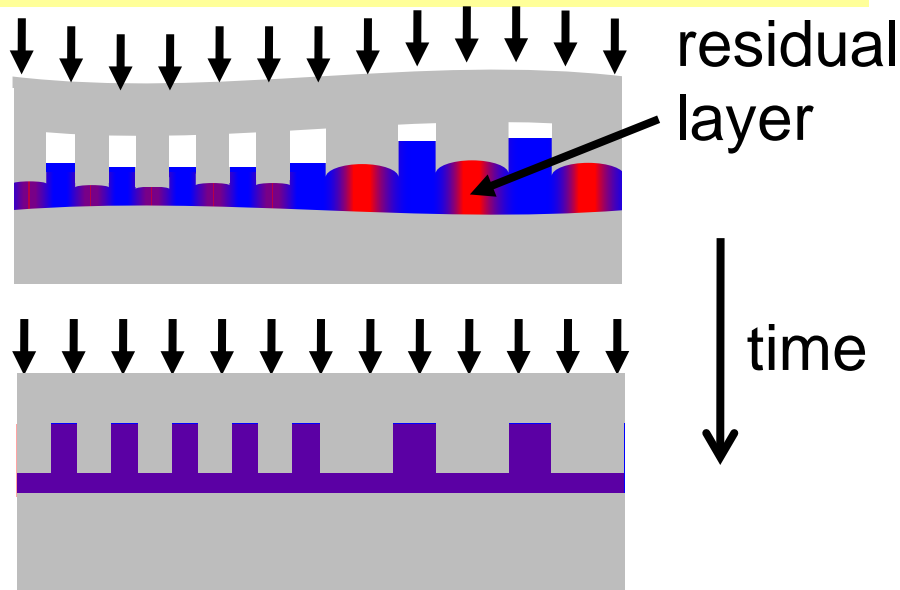
Hayden Taylor and Duane Boning

Massachusetts Institute of Technology



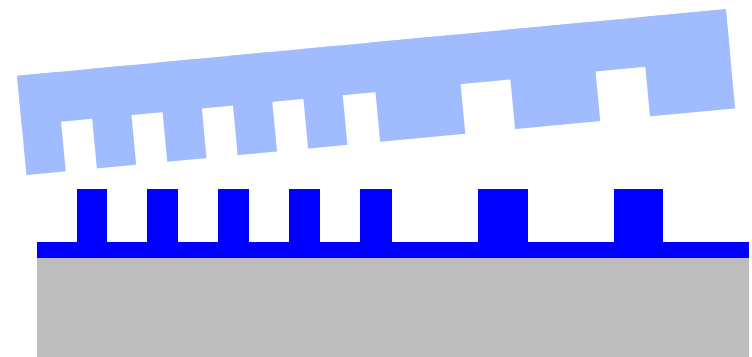
# Nanoimprint is the mechanical patterning of resist spun or sprayed on to a wafer

## Spun-on resist



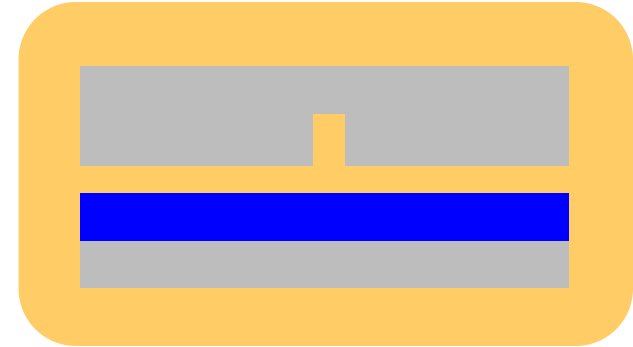
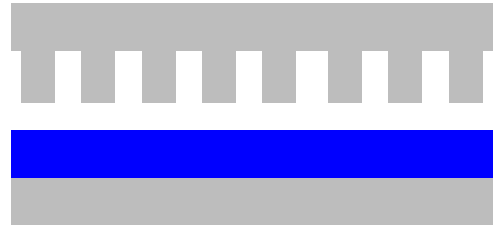
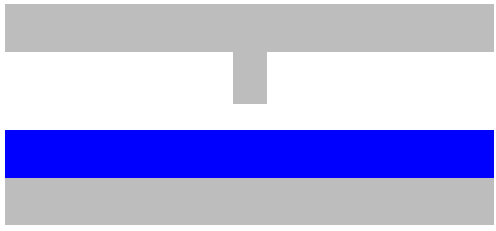
- Resist viscosity  $\geq 10^3$  Pa.s
- Applied pressures  $\sim 5$  MPa
- Thermoplastic or UV-curing
- Viscous resist squeezing
- Elastic stamp deflections

## Droplet-dispensed resist

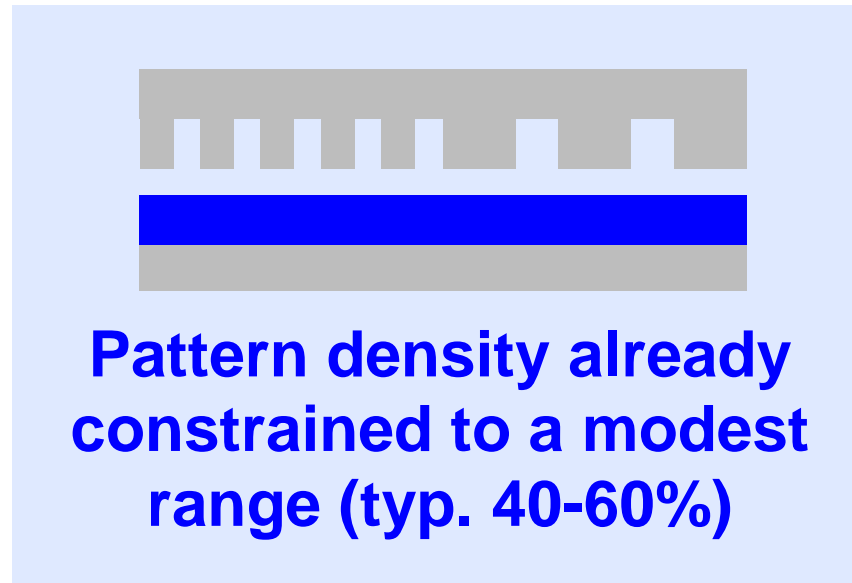


- Resist viscosity  $< 0.1$  Pa.s
- Applied pressures  $\sim 5$  kPa
- Droplets tailored to pattern
- Key figure of merit: filling time
- Gas trapping and dissolution

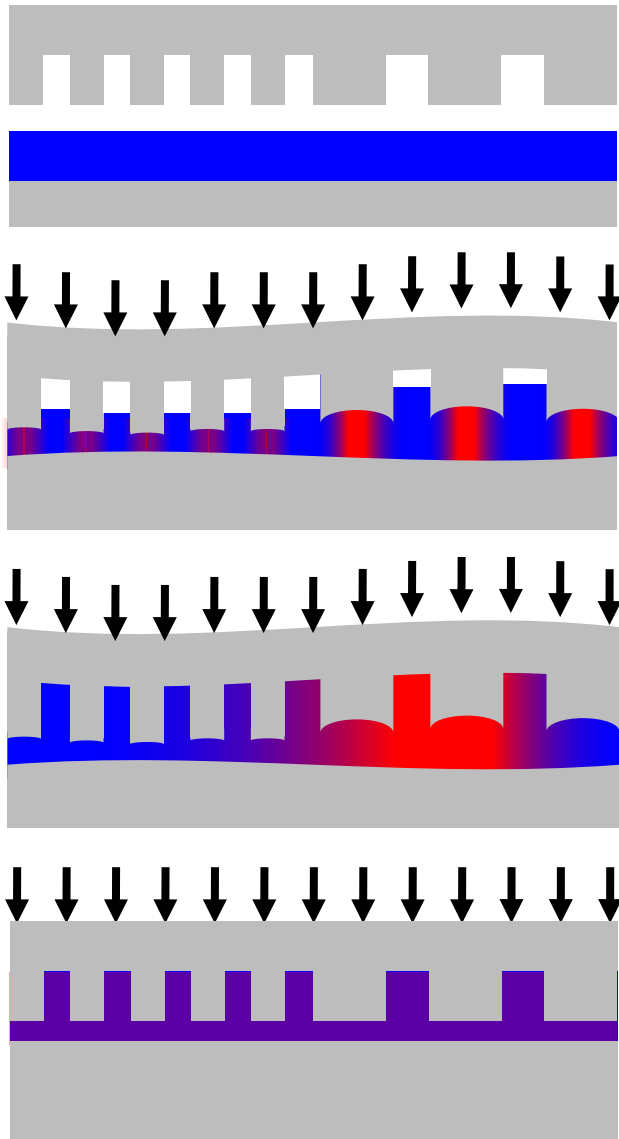
# Nanoimprinting of spun-on layers exhibits pattern dependencies



**Not realistic  
in semiconductors**



# Nanoimprinting of spun-on layers exhibits pattern dependencies

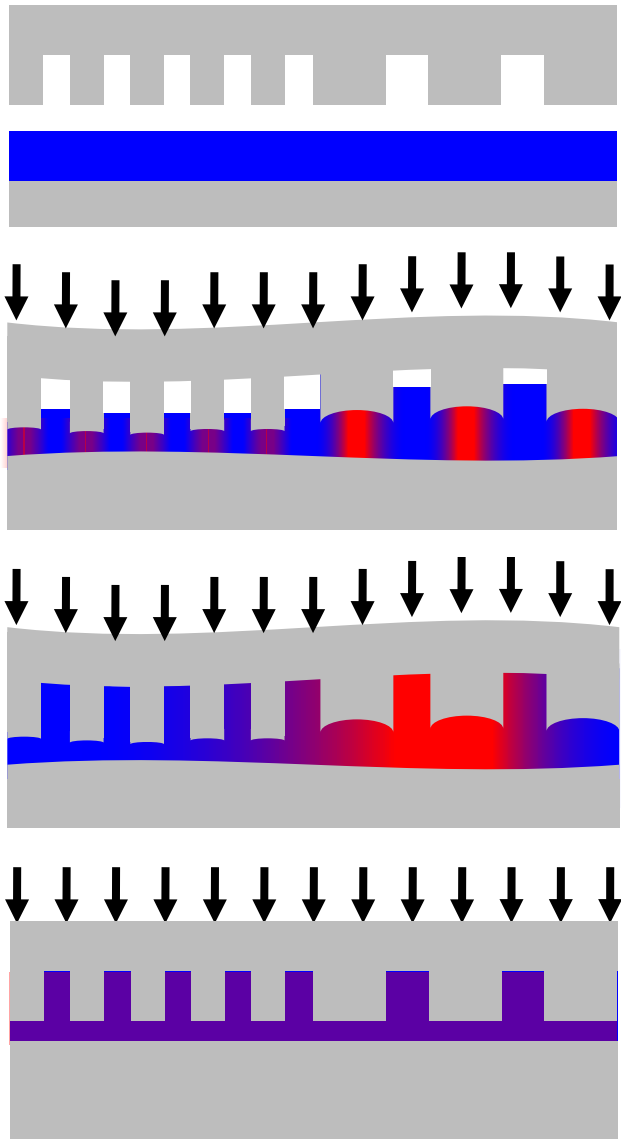


Two relevant timescales for pattern formation:

Local cavity filling

Residual layer thickness (RLT) homogenization

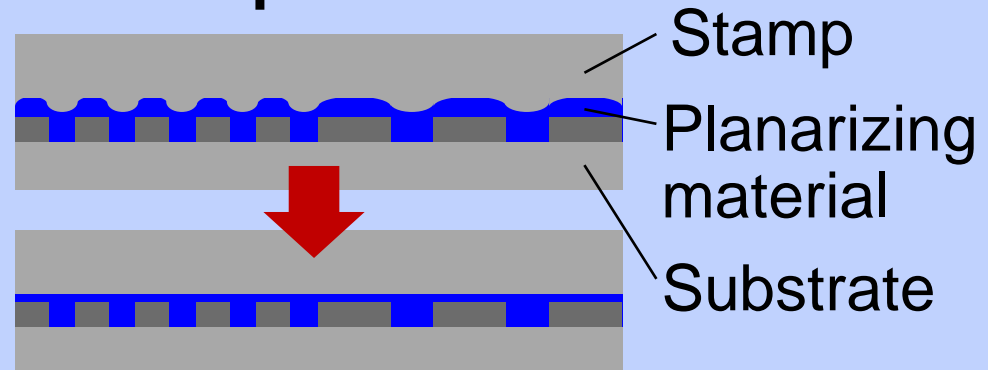
# Nanoimprinting of spun-on layers exhibits pattern dependencies



**Objective for nanoimprint-friendly design:**

*Limit time to bring residual layer thickness variation within spec.*

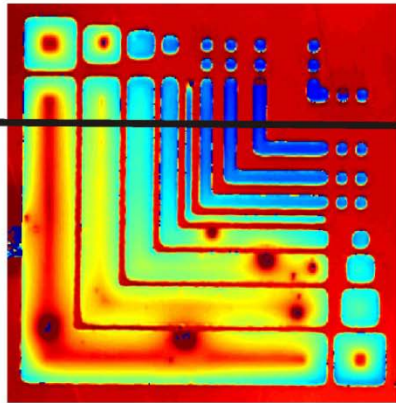
**NIL for planarization**



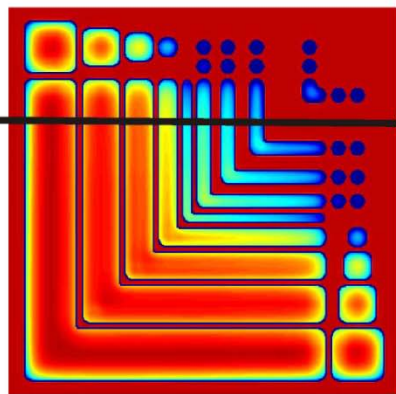
*Similarly, limit time to bring NIL-planarized surface within spec.*

# Nanoimprint modeling and simulation needs

## Experiment

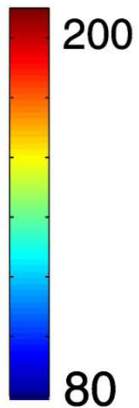


## Simulation



— 0.1 mm

RLT  
(nm)



- **Cell-level**
  - Hundreds of features
  - Guide iterative layout design
  - Desktop processing in minutes
- **Chip-level**
  - Many millions of features
  - Pre-fabrication check: overnight?
  - Guide process selection
- **Need for flexibility**
  - Rapid innovation in resist and stamp materials
  - Richness of geometries

# Nanoimprint compared to photolithography modeling

|               | Photolithography   | Nanoimprint   |
|---------------|--------------------|---|
| Feature-scale | PROLITH;<br>“TCAD” | Hirai <sup>1</sup> ;<br>Rowland <sup>2</sup> ;<br>Scheer <sup>3</sup> ;<br>Reddy <sup>4</sup> |
| Chip-scale    | OPC<br>software    | Mendels/Zaitsev <sup>5</sup> ;<br><i>and this work</i>  |

[1] Y. Hirai *et al.*, *Microelectronic Eng.* vol. 85 p. 842, 2008.

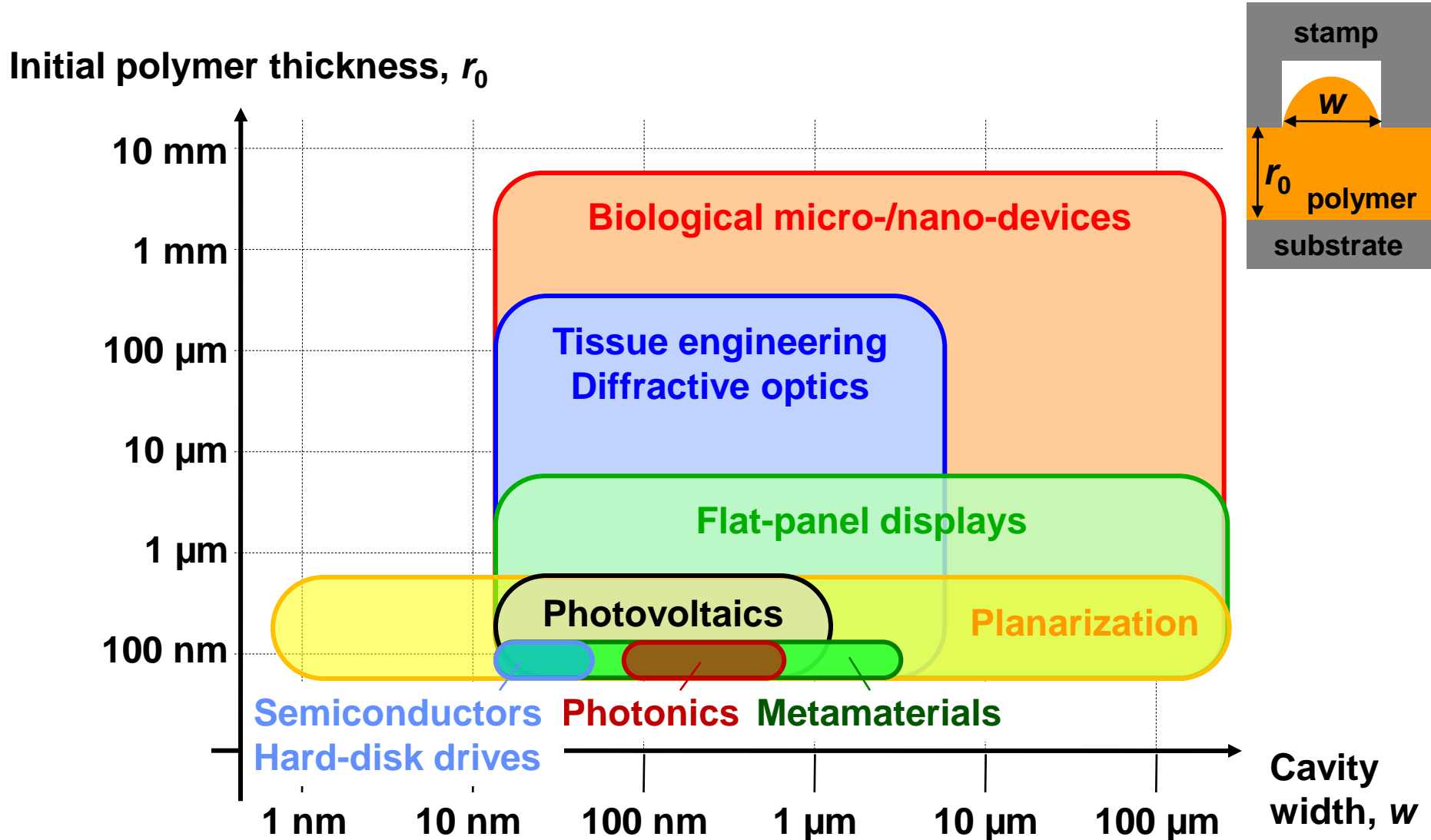
[2] H.D. Rowland and W.P. King, *J Micromech Microeng*, vol. 15, p. 1625, 2004.

[3] H-C. Scheer *et al.*, *Microelectronic Eng.*, vol. 84, p. 949, 2007.

[4] S. Reddy *et al.*, *Phys. Fluids*, vol. 17, p. 122104, 2005.

[5] N. Kehagias *et al.*, *Microelectronic Eng.*, vol. 85, p. 846, 2008.

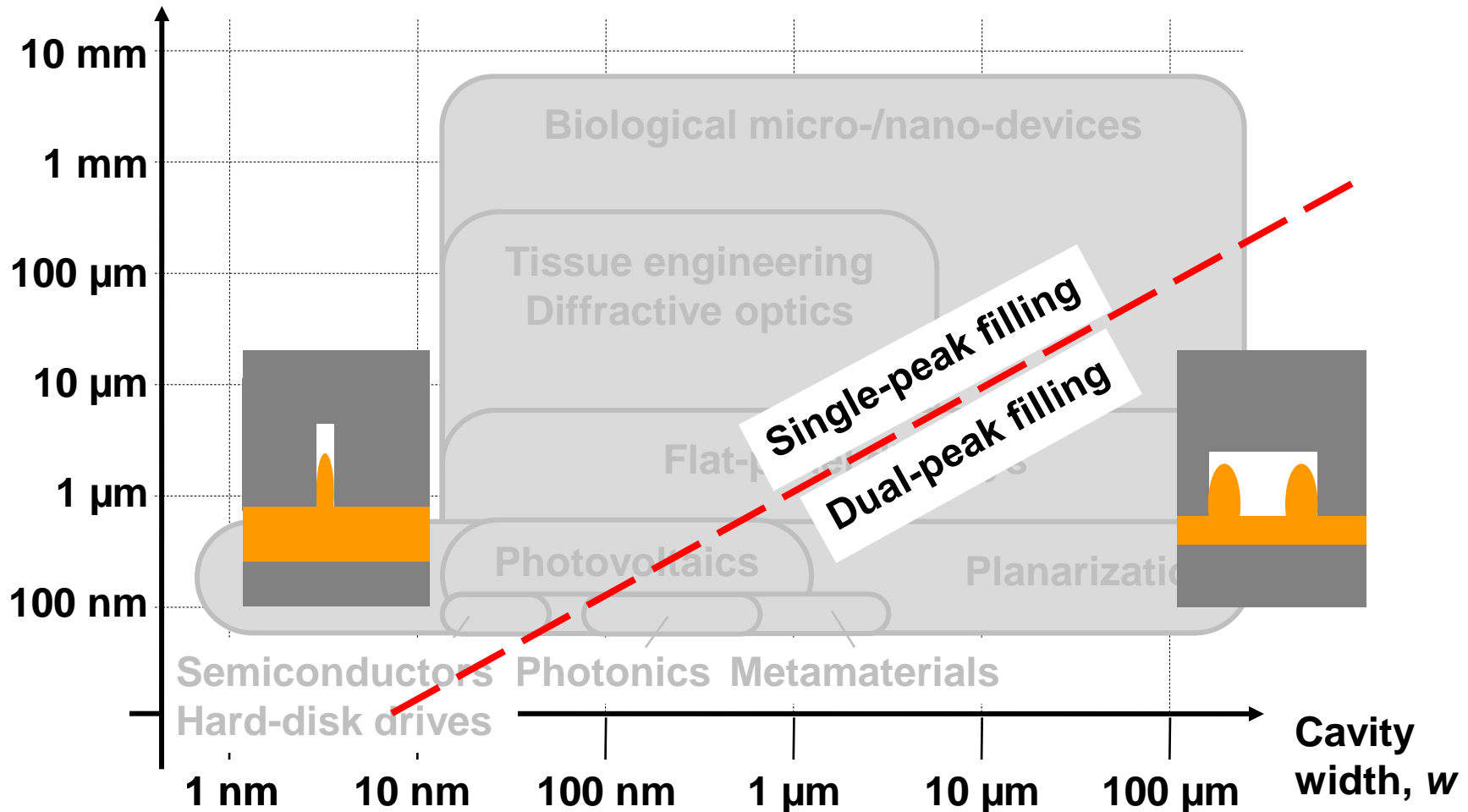
# We need a unified simulation approach for micro- and nano-embossing/imprinting





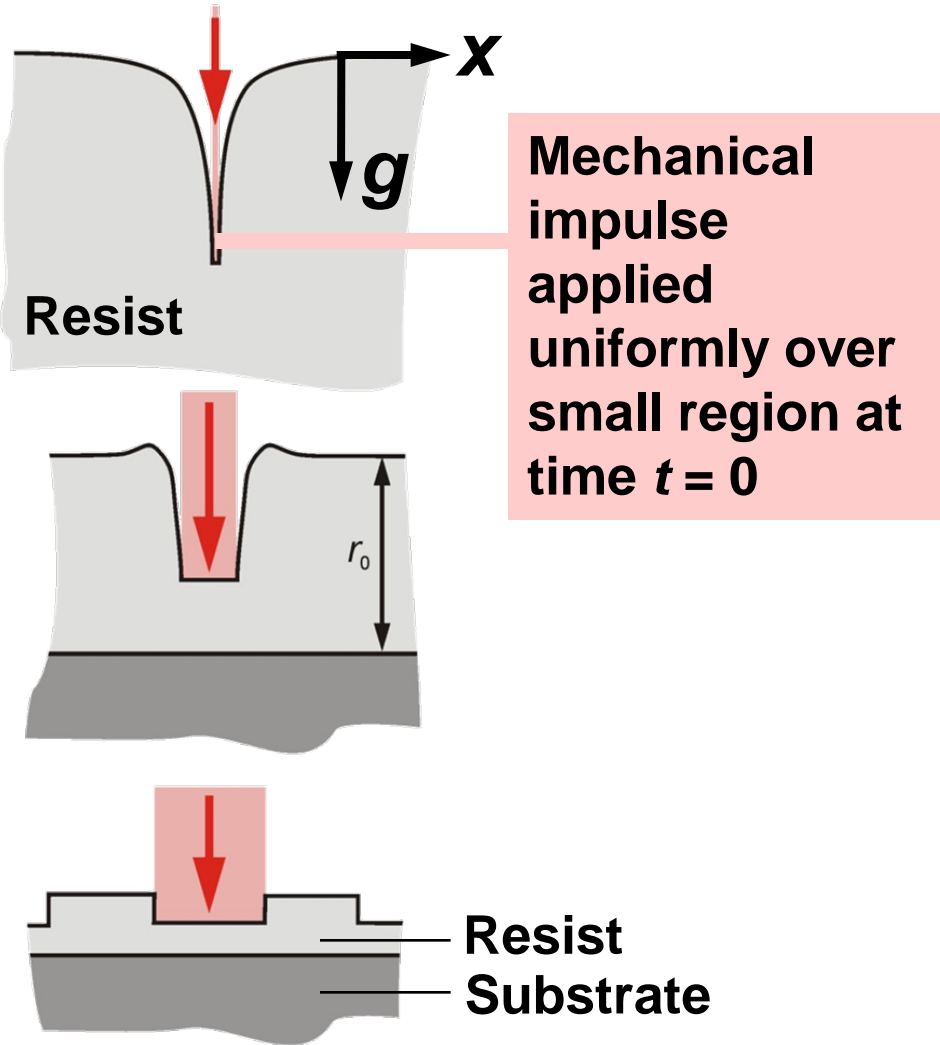
# We need a unified simulation approach for micro- and nano-embossing/imprinting

Initial polymer thickness,  $r_0$

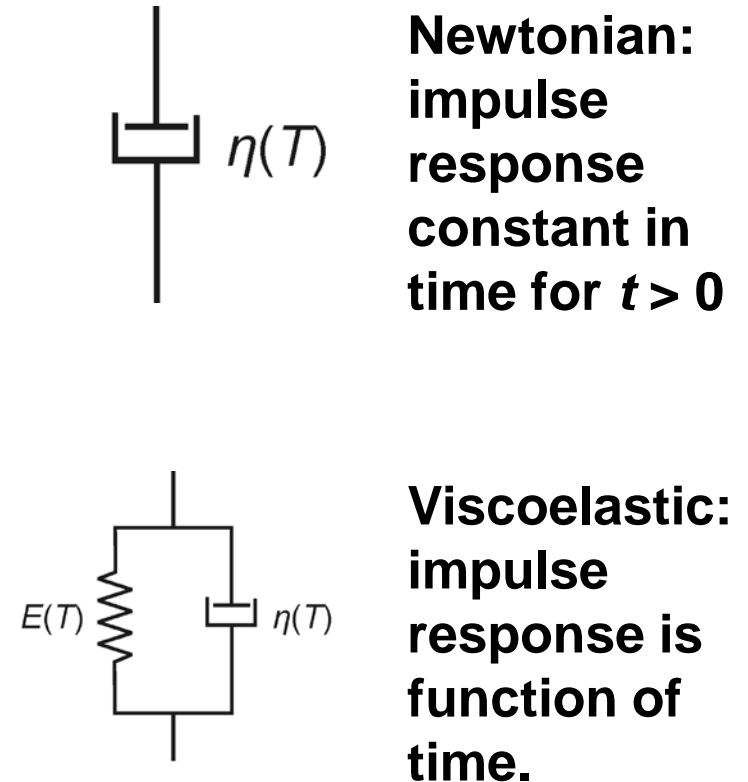


# Key: model impulse response $g(x,y,t)$ of resist layer

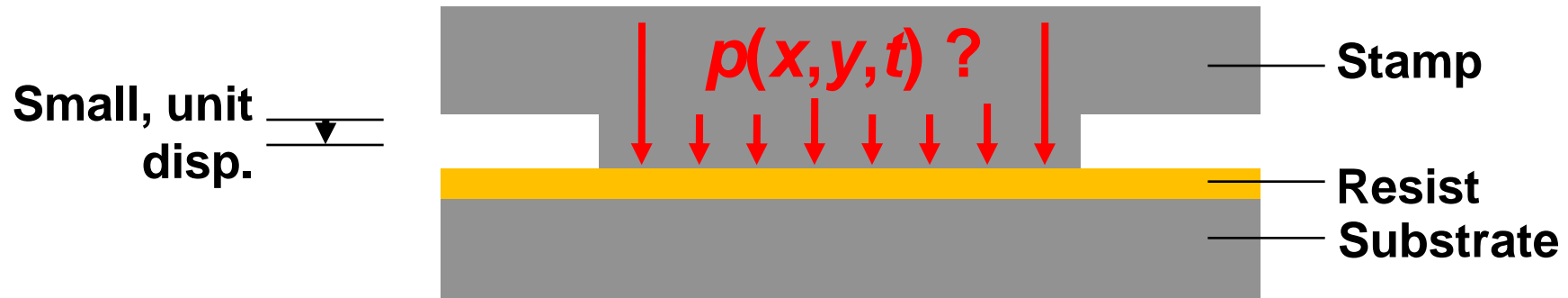
## Model in space:



## Model in time:



# Change in topography is given by convolution of impulse response with pressure distribution



Time increment

$$\left[ p(x, y, t) * g(x, y, t) \right] \Delta t = \mathbf{1}$$

Pressure

?

Impulse response

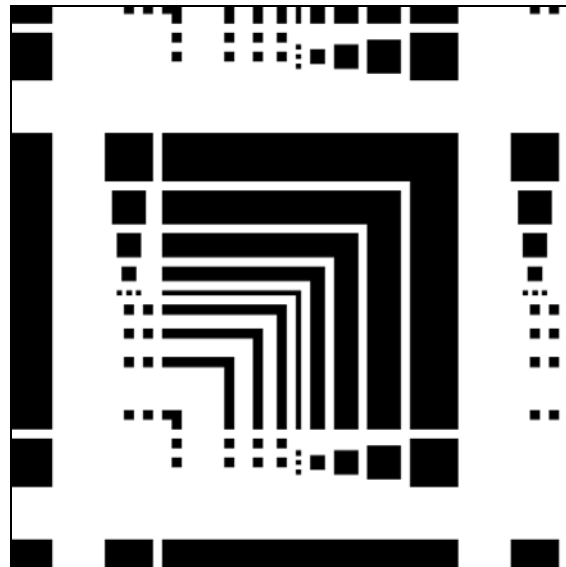
Impulse response

Unit displacement in contact region

# Contact pressure distributions can be found for arbitrary stamp geometries

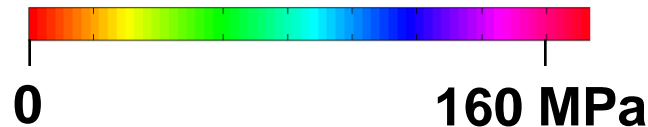
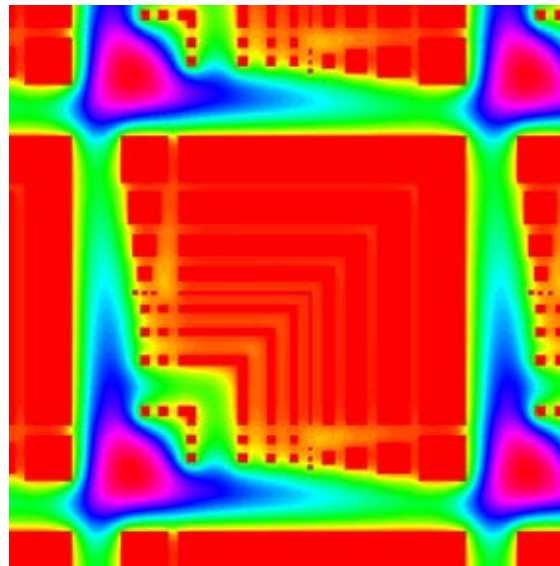
2.3  $\mu\text{m}$ -thick polysulfone film embossed at 205  $^{\circ}\text{C}$  under 30 MPa for 2 mins

Stamp design

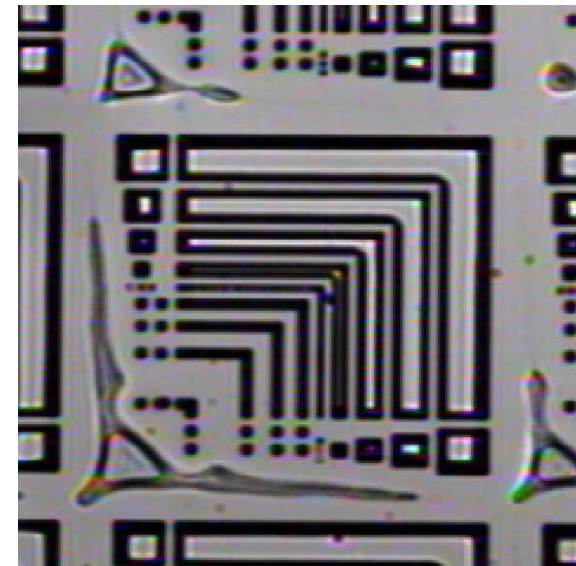


■ Cavity

Simulated pressure



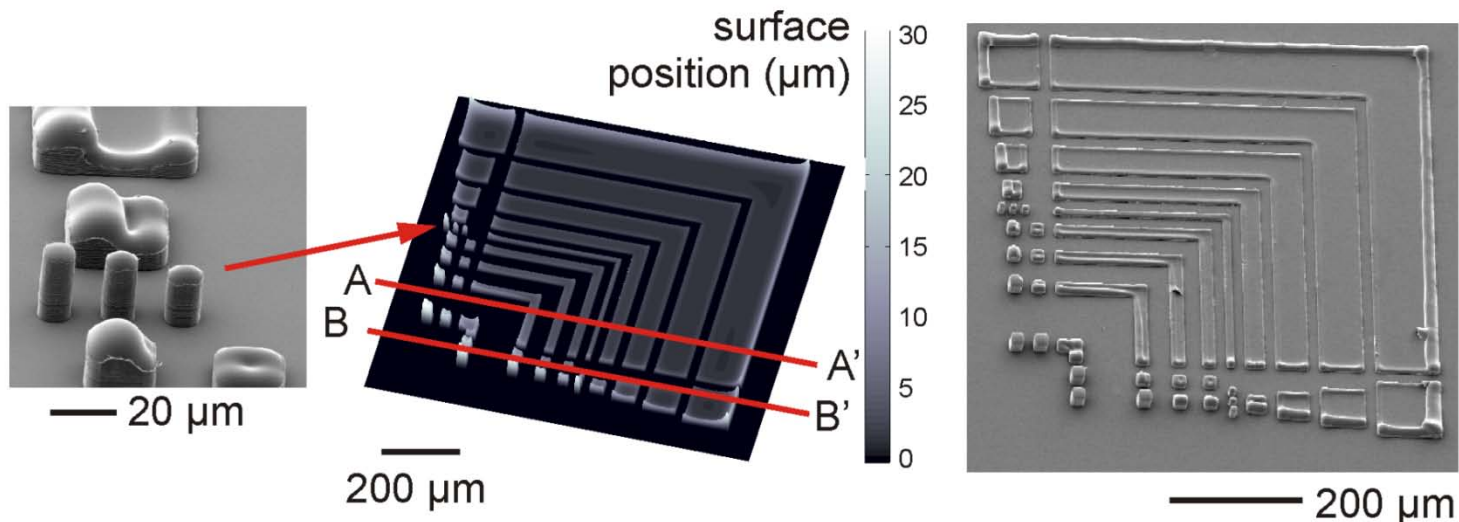
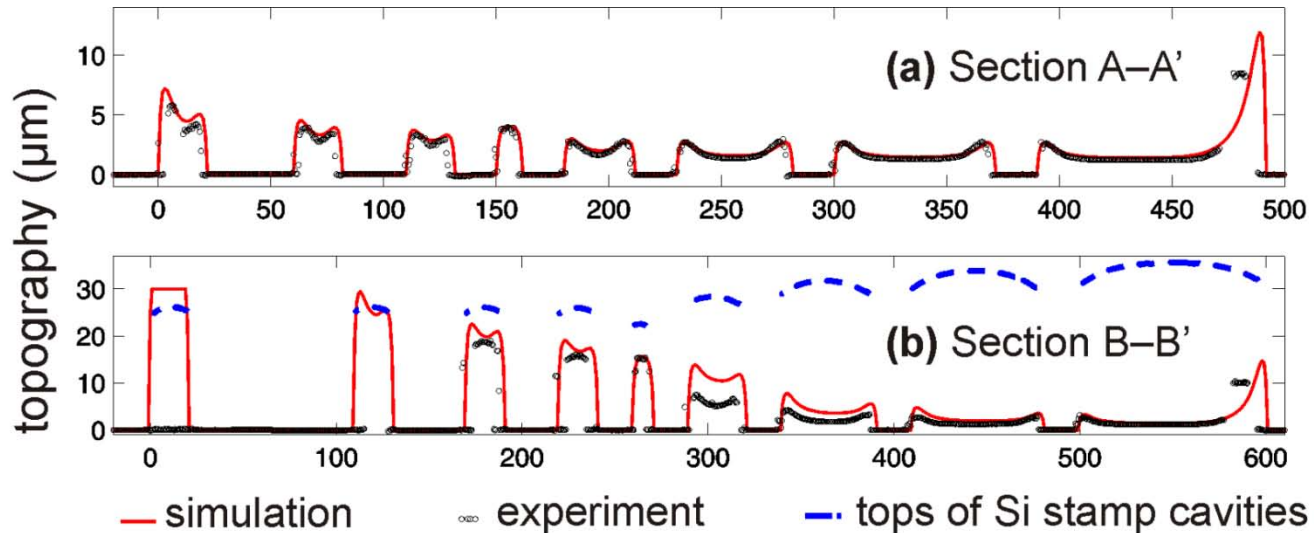
Optical micrograph



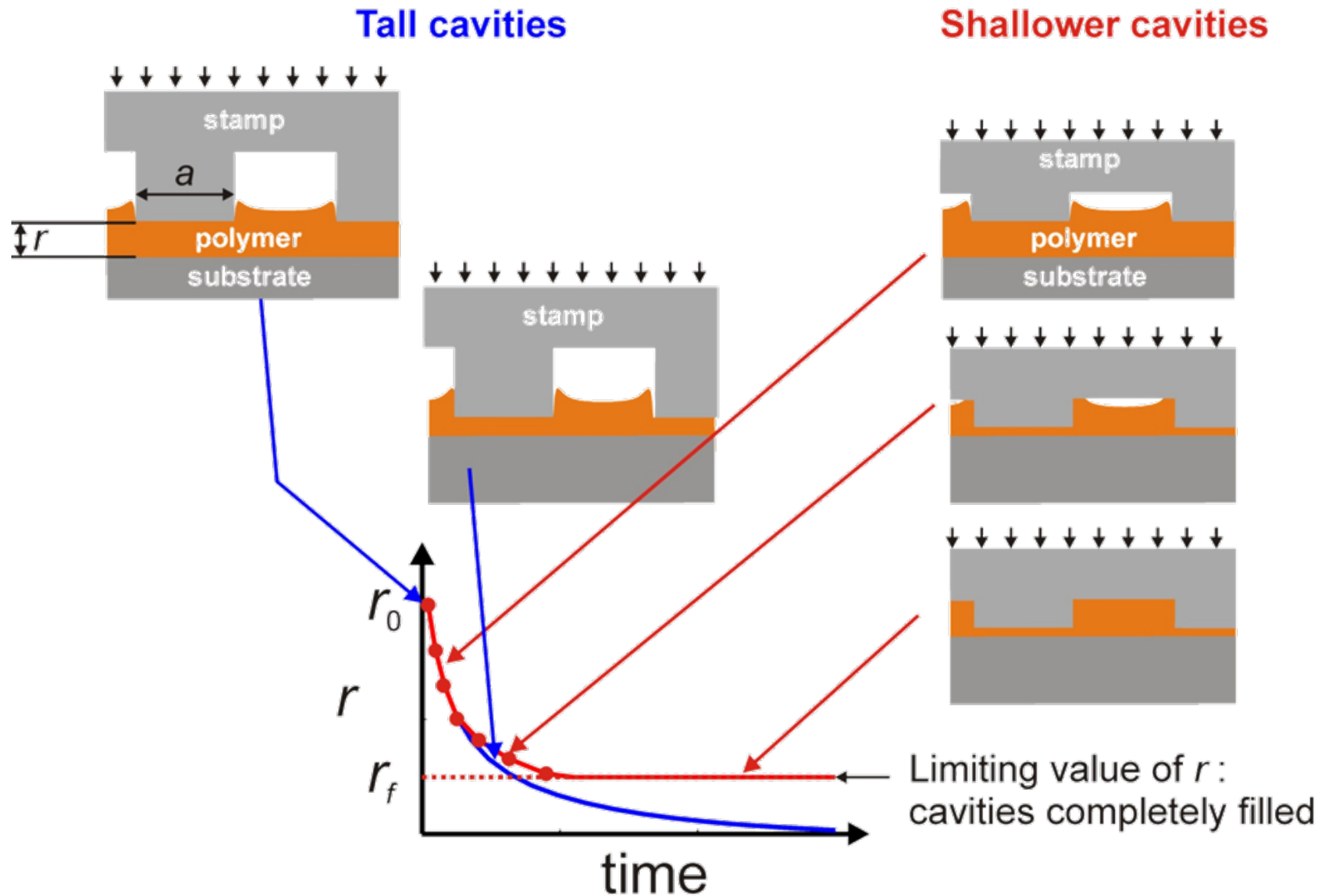
— 200  $\mu\text{m}$

# Successful modeling of polysulfone imprint

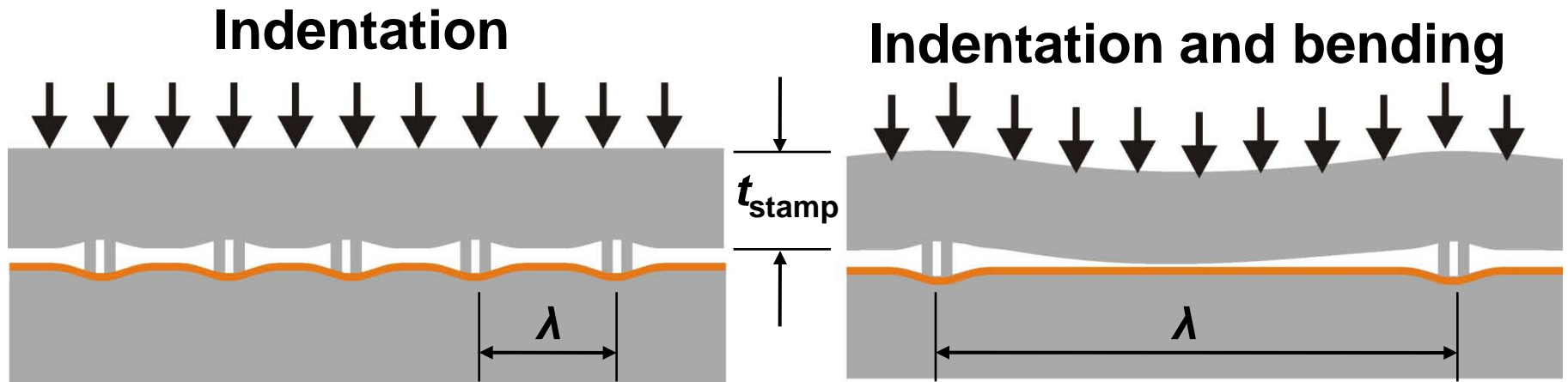
2.3  $\mu\text{m}$ -thick polysulfone film embossed at 205  $^{\circ}\text{C}$  under 30 MPa for 2 mins



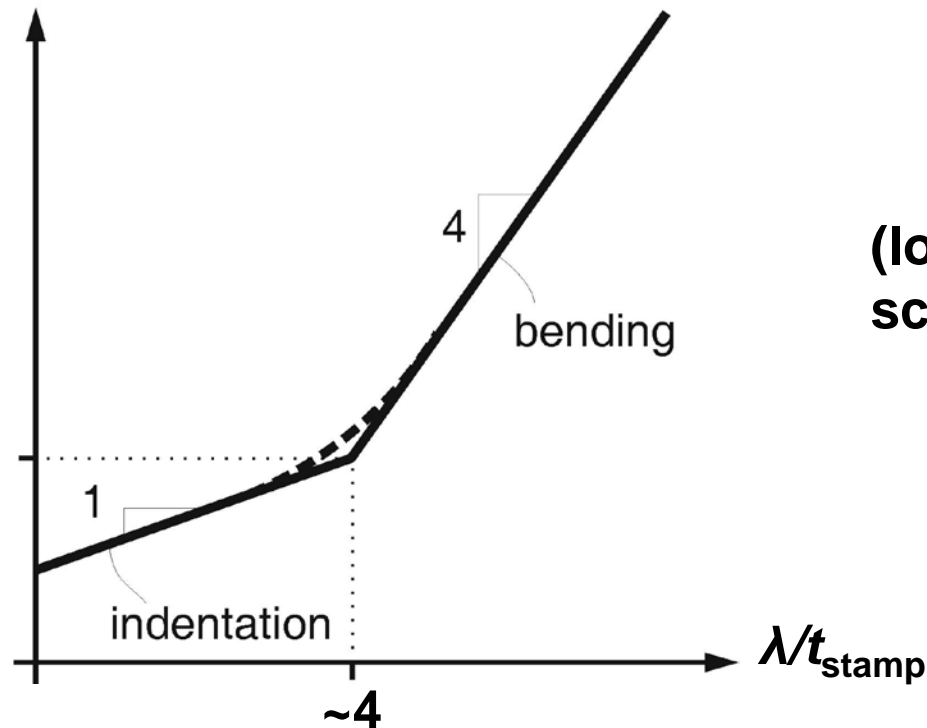
# Representing layer-thickness reductions



# Modeling stamp and substrate deflections



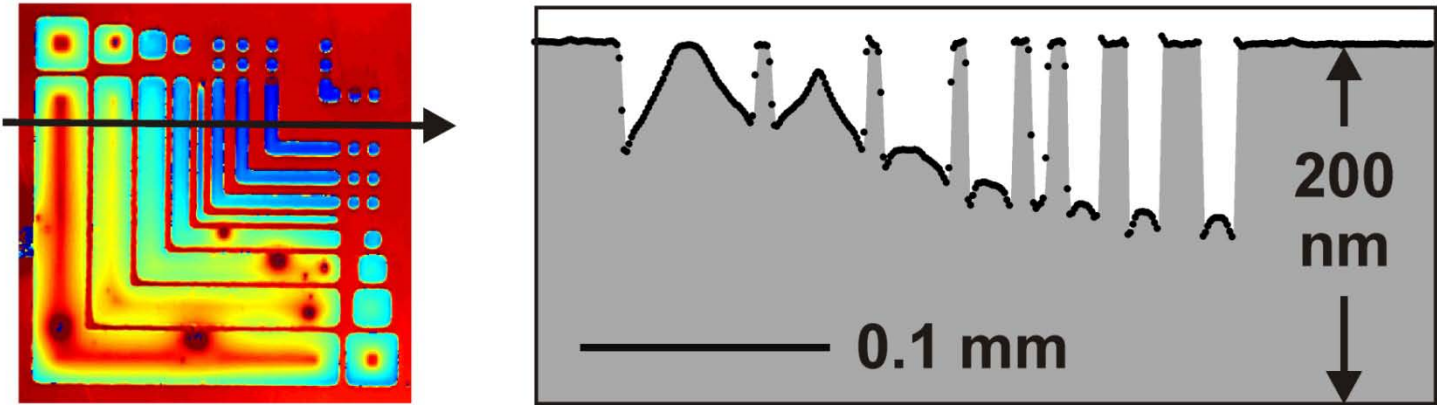
Magnitude of stamp deflection



# Simulation method: step-up resist compliance

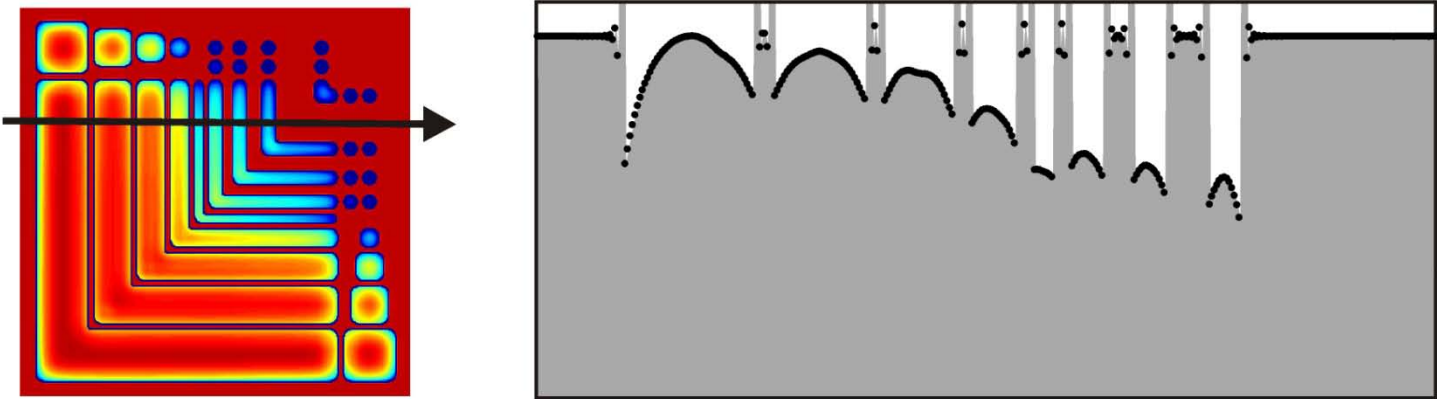
PMMA 495K, c. 165 °C, 40 MPa, 1 min

Experiment



Simulation

RLT (nm)  
200  
80

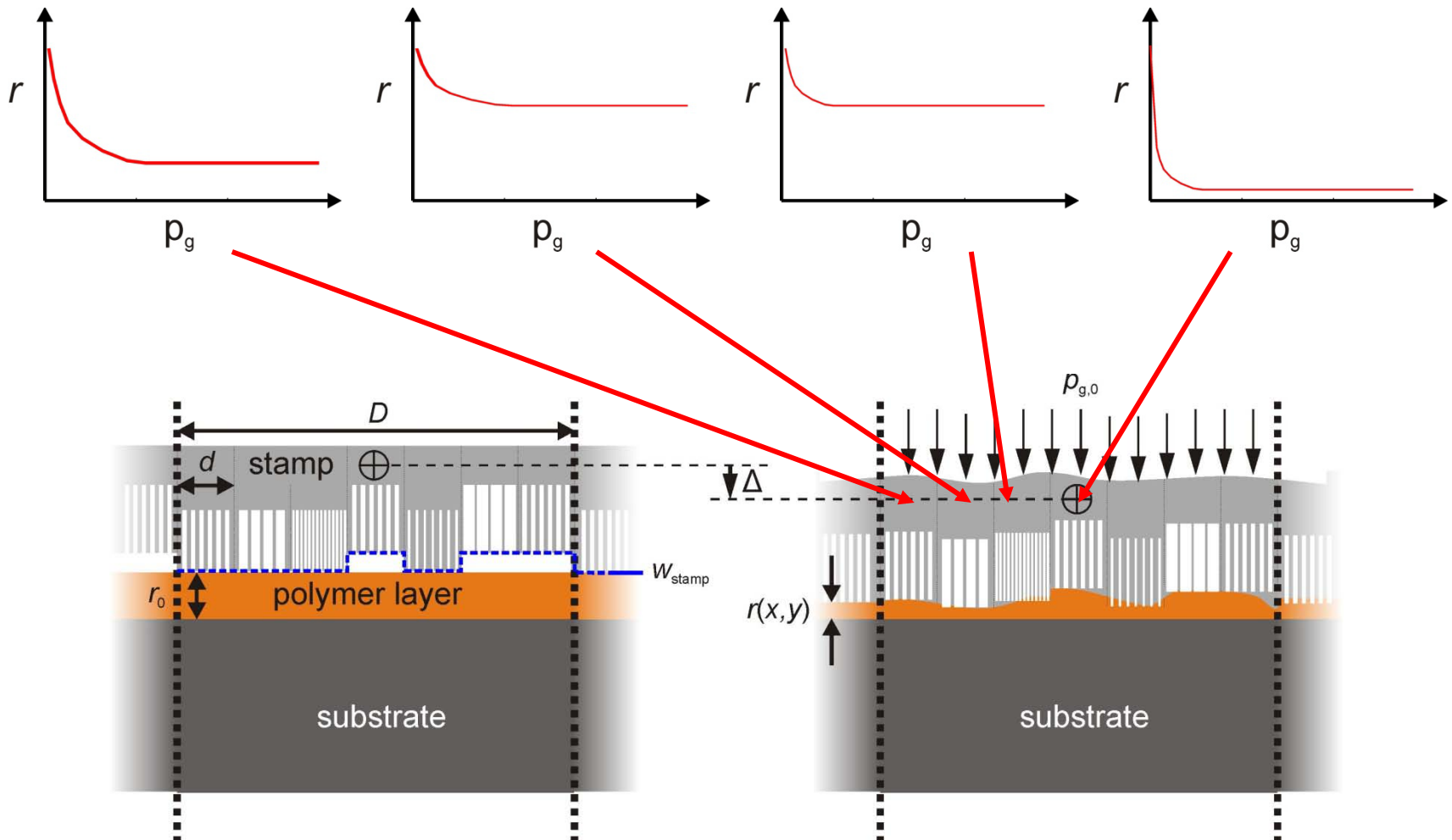


0.1 mm



# Abstracting a complex pattern

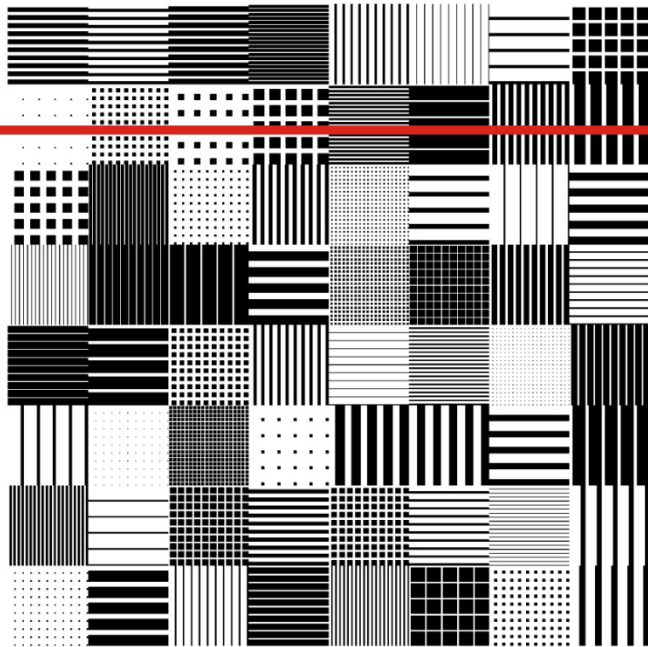
## Local relationships between pressure-compliance and RLT:



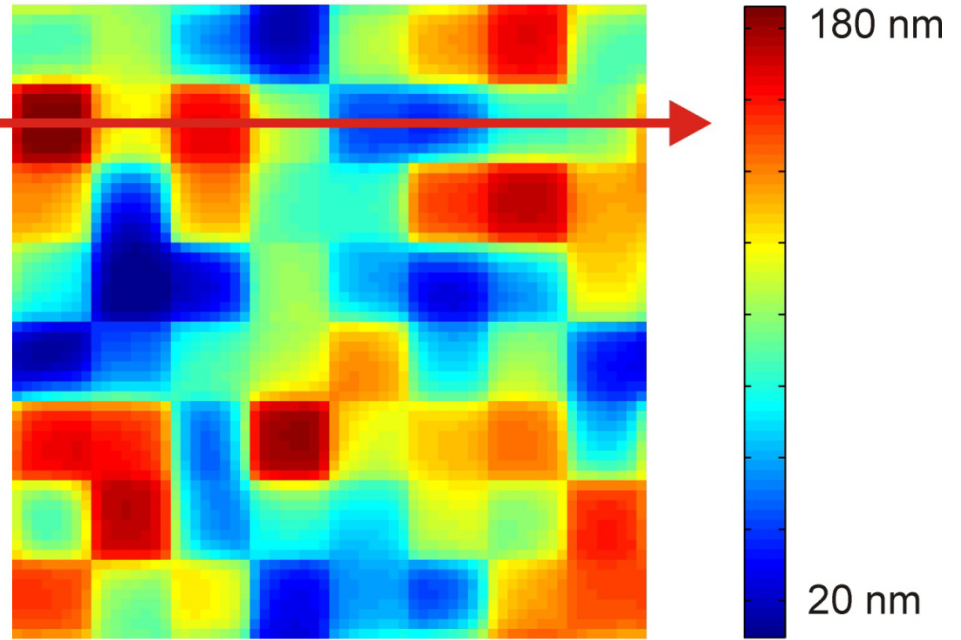
# Simulation results: abstracted pattern

Test-stamp pattern

■ cavity

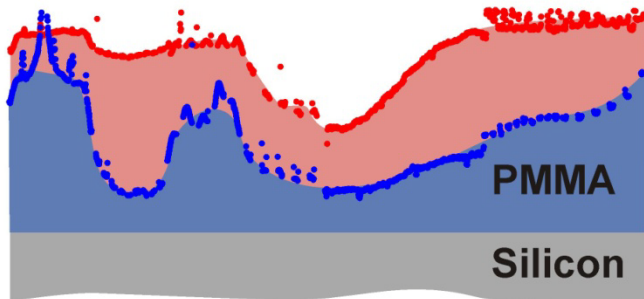


Simulated residual layer thickness



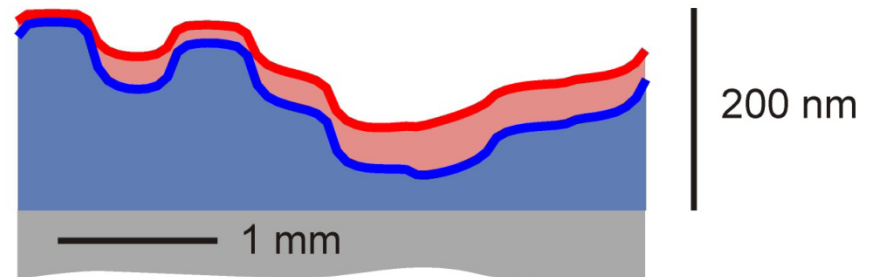
Experimental topography

495K PMMA, 10–15 MPa, 170 °C



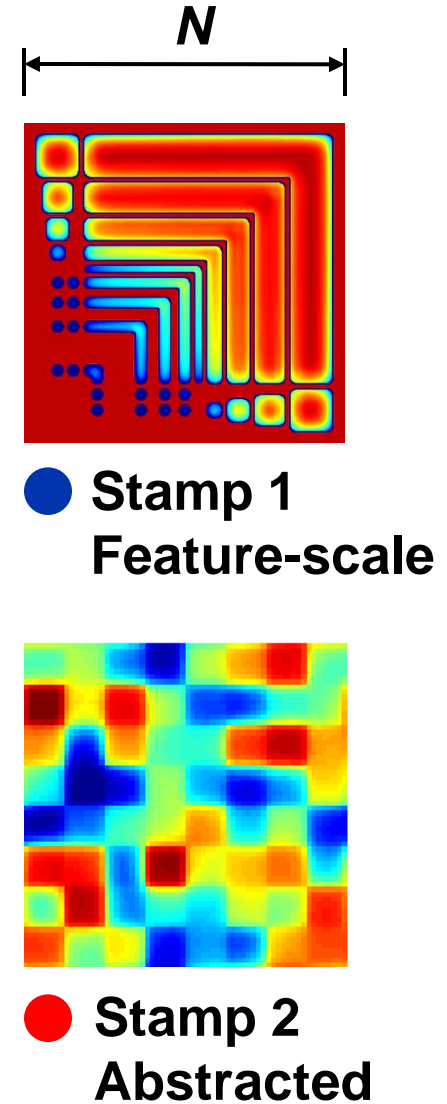
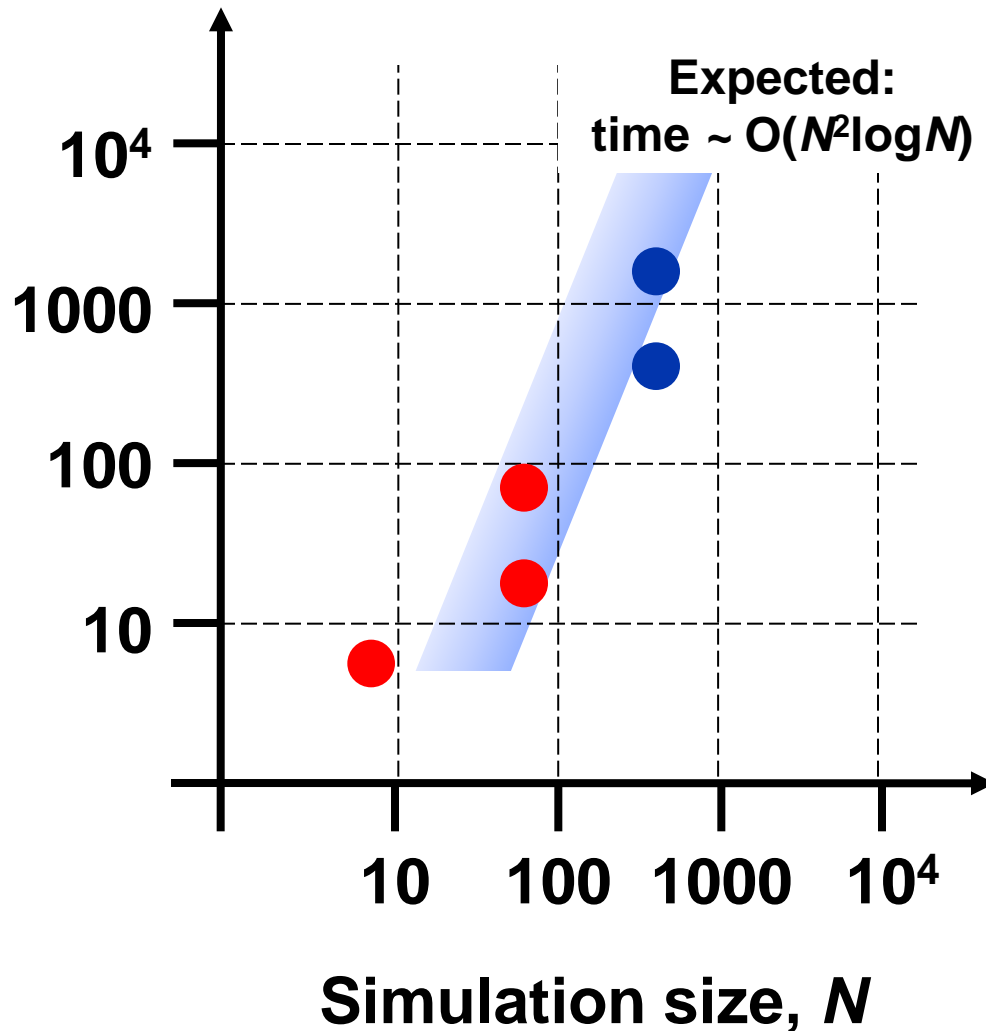
Simulation

3 min  
5 min



# Simulation time

Simulation time (s)



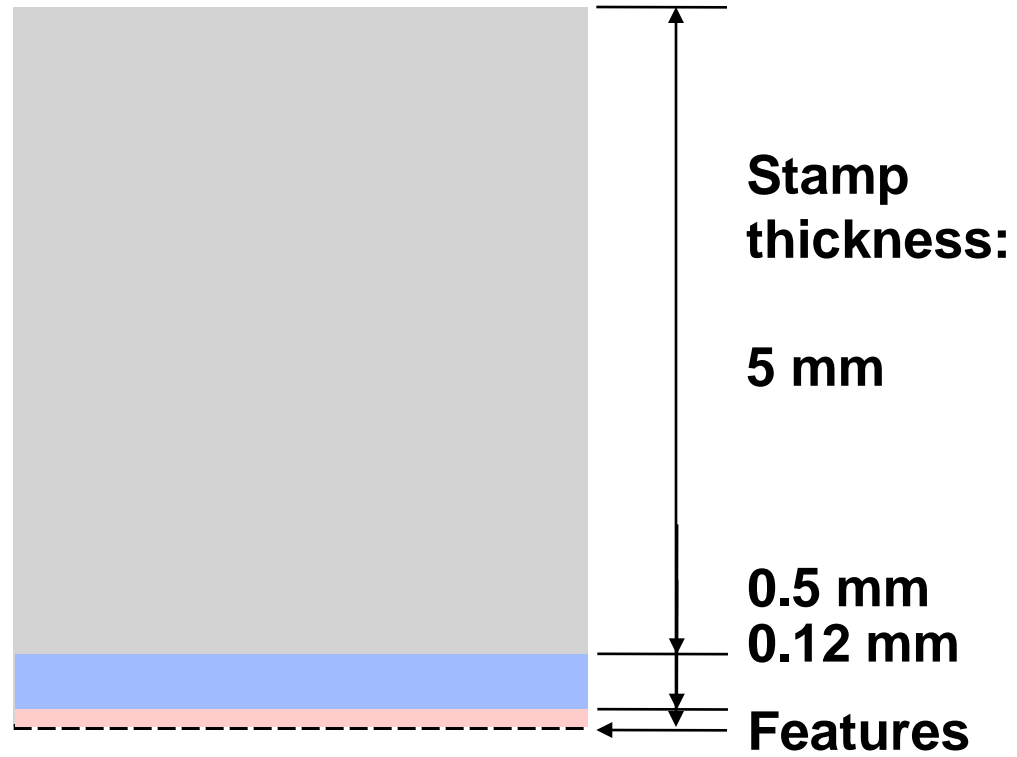
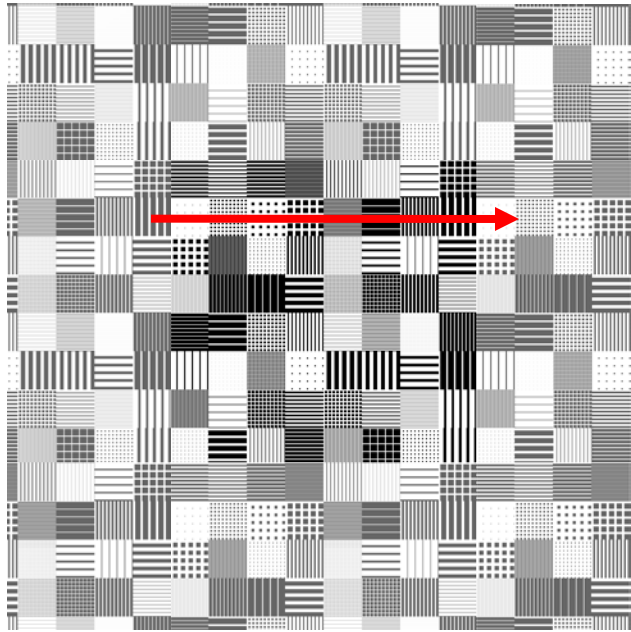
# The physical insights of simulation can be encapsulated in design rules

- **Keep protrusion density  $\rho$  uniform**
  - Dummy fill insertion
  - Importance *grows* with lateral length-scale (unlike CMP)
  - Could vary cavity *heights* spatially\*: expensive
- **Minimize *transient* stamp deflections: uniform  $F_1\rho a^2$** 
  - Care to avoid capillary bridging<sup>+</sup> if some cavities unfilled
  - Impose upper limit on  $F_1\rho a^2$  to limit filling time
  - Trenches quicker to fill than square holes => impose grid
- **Link to other process steps**
  - Exploit RLT variation to counteract etch nonuniformity
- **Pattern density rules, RLT variation target, stamp flexibility and substrate/stamp smoothness will be interrelated**

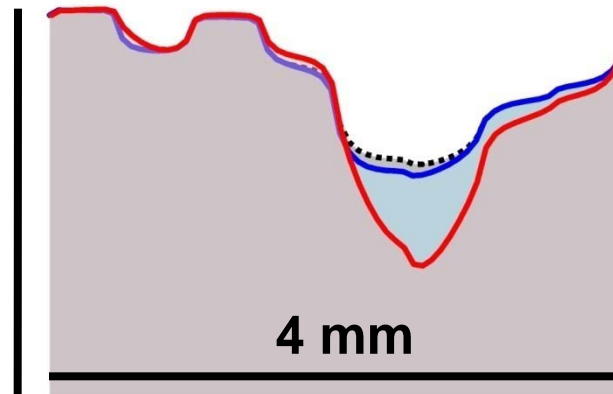
\* H. Hiroshima, in *Proc. Micro- and Nano-Engineering*, 2008.

+ Landis et al., *Microelectronic Eng.*, vol. 84, p. 940, 2007.

# Varying stamp's bending stiffness: simulations



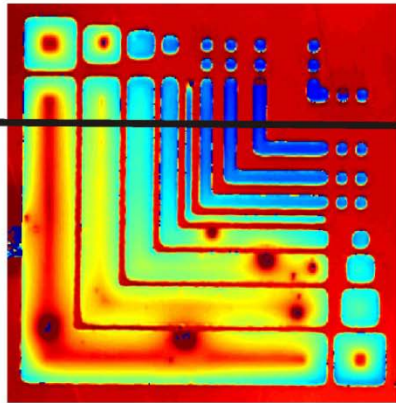
200 nm



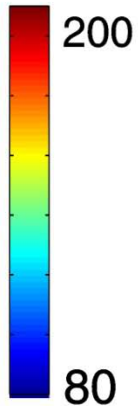
Residual  
layer  
thickness

# Summary: fast nanoimprint modeling

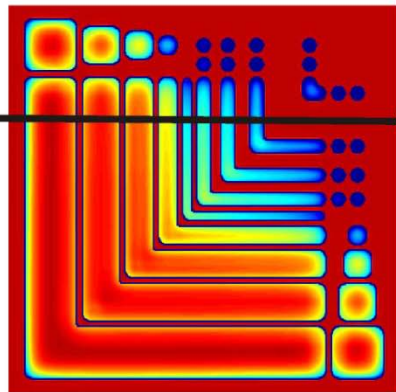
## Experiment



RLT  
(nm)



## Simulation



— 0.1 mm

- **Contributions**

- Flexible modeling approach
- Pattern abstraction optional
- Suited to cell and chip scales
- 1000+ times faster than finite element modeling

- **Outlook**

- We will need NIL-aware design checking
- Can use as an engine for “Mechanical Proximity Correction”

# Acknowledgements

- **Funding**
  - The Singapore-MIT Alliance
- **Colleagues**
  - Matt Dirckx, Eehern Wong, Melinda Hale, Aaron Mazzeo, Shawn Chester, Ciprian Iliescu, Bangtao Chen, Ming Ni, and James Freedman of the MIT Technology Licensing Office
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  - Derek Bassett, Roger Bonnecaze, Siddharth Chauhan, Grant Willson, Yoshihiko Hirai, Wei Wu, Roger Walton, John Mutkoski, Kristian Smistrup, Marc Beck, Andrew Kahng, and Dave White.