Modeling the enhancement of NIL stamp-bending compliance by backside grooves: mitigating the impact of wafer nanotopography on residual layer thickness

Hayden Taylor^{1*}, Kristian Smistrup²⁺, and Duane Boning¹

¹ Microsystems Technology Laboratories, Massachusetts Institute of Technology Room 39-328, 77 Massachusetts Avenue, Cambridge, MA, 02139, USA * hkt@mit.edu

² NIL Technology, Diplomvej 381, DK-2800 Kongens Lyngby, Denmark *ks@nilt.com

Abstract

We describe a model for the compliance of a nanoimprint stamp etched with a grid of backside grooves. We integrate the model with a fast simulation technique that we have previously demonstrated, to show how etched grooves help reduce the cross-wafer residual layer thickness (RLT) variations caused by random undulations of the stamp and substrate wafer topographies.

1. Motivation

- Wafer-scale nonuniformity of residual layer thickness (RLT) remains a challenge in thermal nanoimprint lithography (TNIL).
- The use of backside grooves etched into a silicon stamp [1] can provide long-range flexibility to conform to stamp nanotopography, while retaining short-range stamp rigidity to limit pattern-dependencies.
- The compliance of such stamps needs • to be modeled to enable selection of groove geometries.
- Aim: achieve adequate stamp compliance without making fabrication unnecessarily difficult or consuming a great deal of silicon area with unnecessarily wide flexures.

2. Modeling grooved stamp deflections

Our semi-analytical model for the elastic deflections of a structured stamp captures local indentation, transverse shearing, and bending. The model has been calibrated against finite-element simulations for ranges of initial wafer thicknesses and groove widths and depths.

Right: geometry of NIL stamp with backside grooves. Each square chip sits on a 'mesa' which protrudes ~ 1 μ m from the stamp.

Stamp compliance is considerably increased by backside grooves. 'Compliance enhancement factor' is the ratio of peakpeak deflection of the structured stamp to that of a uniformly $t_{\rm m}$ -thick stamp, under identical loadings.



The model is integrated with our existing scheme for fast TNIL simulation [2,3]: an impulse response describes flowing resist and a point-load response encapsulates stamp flexibility [4]. Stamp deflections, $w_{\rm mesa}$, that would occur with a uniformly $t_{\rm m}$ thick stamp are superimposed on w_{ac} , an approximation to the additional stamp deformation afforded by the grooves.



3. Propagation of parasitic nanotopographies to RLT variation: simulations incorporating a measured wafer topography

4. Limiting systematic residual layer thickness variation



- Measurements of the surface roughness of three virgin silicon wafers (above) show that the amplitude of nanotopography is approximately proportional to its wavelength up to scales of ≥ 10 mm.
- We simulated a thermal NIL process (right) in which the stamp was assumed to have the topography measured from the SSP wafer.
- Simulations indicate that etched backside grooves in the stamp allow the stamp to conform more easily to the substrate, enabling substantial reductions in both mesa-to-mesa



A structured stamp with narrow flexures separating thicker feature-carrying mesas gives smaller systematic RLT variation than a uniformly thin stamp.



 ρ : protrusion density. Resist viscosity fit: 2×10⁵ Pa.s (within the range of literature values for this 50K) PMMA). $t_m = 525 \ \mu m$; $t_a = 150 \ \mu m$; $s_m = 1.5 \ mm$; g =500 µm. Stamp-average pressure 0.35 MPa; imprint time 5 min.

Outlook

and within-mesa RLT variation,
compared to a grooveless stamp of
the same original thickness.

Meanwhile, the ability of grooves mechanically to 'decouple' adjacent mesas with differing protrusion pattern densities is investigated in our recent work [6].

nis table summ neasured stamp om (d) above, LTs, extracted	p topography, extracted and variation of simulated from the three cases in (e).	Mean <i>within</i> - mesa std. dev. (nm)	Mesa-to- mesa std. dev. (nm)
Undeforme	ed stamp topography	1.8	10.4
	<i>t</i> _g = 100 μm	1.0	0.3
Simulated RI Ts	<i>t</i> _g = 150 μm	1.1	0.7
TXE TO	no grooves	1.3	2.3

- Structured stamps offer short-range stamp rigidity combined with longer-range flexibility.
- Longer-range flexibility enables stamps to \bullet conform to random stamp/substrate undulations, improving wafer-scale RLT uniformity.
- Our simulation model allows these benefits to be quantified and stamp geometries selected.

We acknowledge funding from the Singapore-MIT Alliance and the Danish National Advanced Technology Foundation. We thank Matthew Dirckx, Eehern Wong, Lam Yee Cheong, Theodor Kamp Nielsen, and Brian Bilenberg for helpful discussions.



References

T. Nielsen, et al., Proc. 18th IEEE Conf. MEMS 2005, pp. 508–511. [1] [2] H. Taylor and D. Boning, Nanoimprint and Nanoprint Technology Conference, 2009. H. Taylor and D. Boning, *Proc. SPIE*, vol. 7641, 764129, 2010. [3] T. Nogi and T. Kato, J. Tribology, Trans. ASME, vol. 119, pp. 493-500, 1997. [4] [5] R.H. Pedersen, et al., J. Micromech. Microeng., vol. 18, p. 055018, 2008. H. Taylor, K. Smistrup and D. Boning, Micro- and Nano-Engineering Conference, 2010. [6]